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SOFT CORES GAIN GROUND

Key Trends Are Higher Speeds, Better Architectures, Configurability

By Tom R. Halfhill {2/18/03-06}

Although 2002 was a soft market for almost everything high tech, including embedded intellectual property (IP), soft microprocessor cores made great strides last year. All the major vendors introduced new or enhanced versions of their leading synthesizable products. Microarchitectures grew more sophisticated; configurability became more popular; benchmark scores broke records; and clock frequencies (largely driven by advances in fabrication technology) zoomed to levels once considered the exclusive domain of hard cores and high-performance embedded chips.

What's even more impressive is that all this progress came in the face of major layoffs, hiring freezes, budget cuts, canceled projects, shuffled priorities, and other distractions of what economists cheerfully refer to as the business cycle. Every IP vendor cut expenses in some fashion, but the most aggressive companies have continued to invest in new product development, hoping to gain a competitive edge when the economy recovers. IP vendors tend to think long-term, anyway, because it takes one to three years for developers to integrate cores into chips and, ultimately, into finished products. That's a long time to wait for a royalty stream to flow. It's a business model difficult to synchronize with quarterly thinking.

What's driving licensable IP is the diversity of the embedded-systems market and the relative health of key market segments. It's nothing like the sluggish PC market, which has coalesced around a couple of slowly changing system architectures that support only two distinct microprocessor architectures from a handful of vendors. The embedded market encompasses everything from MP3 players and videogame consoles to automotive telematics and industrial robots. It's a lively, fast-moving industry that requires and encourages a proliferation of microprocessor architectures from dozens of vendors. And there's additional room for licensable IP cores—the building blocks of ASICs and SoCs optimized for specific products or classes of products.

Our year-end review covers (in alphabetical order) five vendors whose 32-bit processor cores have been nominated for an *MPR* Analysts' Choice Award in the IP Core Processor category: ARC International (formerly ARC Cores), ARM Holdings, Improv Systems, MIPS Technologies, and Tensilica. Table 1 compares the general features of these 32-bit processors.

Missing from this year's roster of IP vendors are Lexra and PicoTurbo. Lexra became a MIPS licensee and stopped licensing its own MIPS-like processor cores after settling a patent lawsuit with MIPS. In early 2003, Lexra dissolved. PicoTurbo suffered a similar fate, virtually disappearing after an unsuccessful legal battle against a patent lawsuit filed by ARM. Another casualty of 2002 was BOPS, which won last year's *MPR* Analysts' Choice Award for Best DSP Core. Although the company still clings to life, massive layoffs have pared it down to a skeleton staff.

ARC Introduces Code Compression

ARC continued its struggle toward profitability in 2002, cruising on a huge pile of cash (currently about $168 million) raised in a successful IPO moments before the tech bubble

popped in the fall of 2000. Despite this cushion, ARC has drastically slashed expenses, laying off scores of employees, consolidating offices, and outsourcing some design projects.

Headed by a new CEO, Mike Gulett (formerly of Globespan/Virata), ARC continues to attract licensees, chalking up more than two dozen design wins in 2002. ARC sold 14 design licenses for its ARCtangent-A5 microprocessor core, the company's most important new product of the year. Prominent new customers include Intel Microelectronics Services, the fabless ASIC unit of Intel, which is offering the ARCtangent processor to third-party chip developers.

ARCtangent-A5 is an enhanced version of the ARCtangent-A4 customizable processor core. It retains the basic features of the A4, including user-configurable instructions, registers, caches, on-chip memories, bus interfaces, interrupts, and peripherals. What's new is the ARCompact instruction-set architecture (ISA), which adds a subset of 16-bit instructions to the 32-bit instruction set. ARCompact can reduce code size in a typical embedded application by 30%, according to ARC.

By itself, a dual-length ISA isn't new, of course. Among processor-IP competitors, ARM has its 16-bit Thumb instructions, MIPS has its MIPS-16e subset, SuperH has its original 16-bit instruction set, and Tensilica's Xtensa processors have always offered a combination of 16- and 24-bit instructions. However, ARCompact takes a slightly different approach, overcoming some disadvantages inherent in other code-compression schemes. (See sidebar, "ARCompact: An Elegant 16/32-Bit ISA.") *MPR* considers ARCompact a significant achievement, so we nominated **ARCtangent-A5** (the first processor to implement ARCompact) for an *MPR* Analysts' Choice Award in the IP Core Processor category.

ARC continued to differentiate itself from its main competitors in 2002 by offering platform IP, not just processor cores. The company introduced a Hi-Speed USB 2.0 host/device peripheral core for ARCtangent-A5, USB On-the-Go IP, and telephony extensions for voice-over-Internet-protocol (VoIP) applications. ARC also offers DSP extensions, DES/3DES-acceleration extensions, a customizable real-time operating system (RTOS), network-protocol stacks, and comprehensive development tools for its processors.

A third-party IP vendor, Digital Communications Technologies (DCT), introduced Java extensions for ARCtangent. These extensions natively execute Java bytecode instructions while adding only 5,000 gates to the processor core—several thousand fewer gates than ARM's similar Jazelle extensions.

In 2003, ARC wants to continue expanding its catalog of platform IP while pursuing its twin financial goals: generating more royalty revenue and turning a profit. Some stockholders are growing impatient, so ARC recently announced it will buy back about half its outstanding shares in 1H03. That would effectively reduce ARC's cash holdings by a like amount and refund the money to stockholders, still leaving the company with a substantial cash reserve.

To compete effectively, ARC must keep developing new products that stand out from the crowd. However, developing and supporting a catalog of platform IP is much more difficult than focusing on processor cores, especially with ARC's layoff-depleted workforce. To fill the gap, ARC is outsourcing more product development and forming alliances with other companies. Still, with so many code bases to develop and support, ARC is stretching itself thinner than companies like ARM, MIPS, and Tensilica, which are more focused on microprocessors and have equal or greater engineering resources.

ARM Stays Muscular Despite Recession

ARM—the world's leading vendor of licensable microprocessor cores—has fared relatively well during tough times, remaining profitable while gaining even more licensees and design wins. However, profits are relatively flat compared with recent years, and even the mighty ARM found it necessary to lay off 12% of its workers to keep expenses in line.

Although the embedded market is too diverse for a single architecture to dominate, ARM is becoming so popular in low-power applications that it's as ubiquitous as the x86 architecture in the PC market.

	ARCtangent-A5 ARC	ARM1026EJ-S ARM	ARM1136JF-S ARM	Jazz-Crescendo Improv	M4K MIPS	Xtensa V Tensilica
Architecture	32-bit RISC	32-bit RISC	32-bit RISC	32-bit VLIW	32-bit RISC	32-bit RISC*
Target Applications	General-purpose embedded	General-purpose embedded	General-purpose embedded	Media processing	General-purpose embedded	General-purpose embedded
Instruction Lengths	16/32 bits	16/32 bits	16/32 bits	32 bits	16/32 bits	16/24 bits
Configurability	High	Low	Low	High	Medium	High
DSP Extensions	Optional	Standard	Standard	Standard	No	Optional
Java Extensions	Third-party	Standard	Standard	No	No	No
MMU	No	Yes	Yes	No	No	Yes
FPU	No	No	Yes	No	No	Optional
Multiple Reg Files	Optional**	No	No	Optional	1–4	Optional**
Cert EEMBC Scores	No†	No††	No	Yes	No	Yes
Availability	Now	Now	Now	Now	Now	Now

Table 1. Except for Improv, whose Jazz cores are more specialized, all these synthesizable microprocessors compete for similar customers and products. *VLIW extensions optional. **Requires HDL coding. †Certified scores are available for the similar ARCtangent-A4. ††Certified scores are available for the similar ARM1020E.

Important Embedded-IP Events of 2002

ARM introduced the next-generation ARM11 microarchitecture at Embedded Processor Forum, revealing more details about the ARMv6 architectural specification announced at Microprocessor Forum 2001 (*MPR 6/3/02-01*, "ARM Family Expands at EPF"). Also at EPF, ARM revealed significant details about its new ARM1026EJ-S, a synthesizable derivative of the ARM1020E hard microprocessor core (*MPR 4/29/02-01*, "Exploring the ARM1026EJ-S Pipeline"). A few months later, at Microprocessor Forum, ARM introduced the ARM1136J-S and ARM1136JF-S, a pair of ARM11 synthesizable cores (*MPR 10/21/02-02*, "MPF Hosts Premiere of ARM1136").

BOPS won the Analysts' Choice Award for Best DSP IP Core of 2001. The BOPS WirelessRay is based on the company's unique VLIW ManArray architecture (*MPR 2/25/02-03*, "Best DSP IP Cores of 2001").

Digital Communications Technologies (DCT) announced its Lightfoot and Bigfoot Java processors, available for licensing as synthesizable cores and also to be offered as chips. Bigfoot is based on the ARCtangent microprocessor core from ARC International; DCT's extensions allow it to natively execute Java bytecode instructions (*MPR 1/28/02-04*, "DCT Marches Into Java Processors").

Improv Systems shipped the Crescendo solution kit with a second-generation customizable media-processor core based on the company's VLIW architecture (*MPR 7/22/02-01*, "Improv Builds to Crescendo").

LSI Logic shipped the ZSP600, a second-generation DSP core based on the earlier ZSP400 (*MPR 3/11/02-02*, "ZSP600 Does Zesty DSP").

MemoryLogix, a startup, announced the MLX1, an x86-compatible synthesizable core for SoC integration. The 32-bit processor is designed for low-power applications (*MPR 11/11/02-02*, "MemoryLogix Makes Tiny x86").

MIPS Technologies introduced the new MIPS32 M4K synthesizable microprocessor core at Embedded Processor Forum (*MPR 5/20/02-01*, "MIPS' Latest Core Goes Multiprocessor"). A few months later, MIPS announced SOC-it, a family of synthesizable system controllers for SoC designs, based on the MIPS 4K, 5K, and 20K cores (*MPR 9/3/02-02*, "MIPS Offers Key SoC Component").

Tensilica shipped Xtensa V, a new version of its customizable soft-microprocessor core. In simulation, Xtensa V achieved the highest EEMBC ConsumerMark score to date (*MPR 9/16/02-01*, "Tensilica Xtensa V Hits 350MHz"). Tensilica also announced its Xtensa processors will support IBM's CoreConnect on-chip bus (*MPR 10/7/02-02*, "Tensilica Adopts CoreConnect Bus"). Another Tensilica announcement was FLIX (flexible-length instruction extensions), which adapts VLIW concepts for communication, multimedia, and networking applications (*MPR 11/25/02-06*, "FLIX: The New Xtensa ISA Mix"). And in November, Tensilica won three new U.S. patents for its configurable-CPU technology (*MPR 12/9/02-01*, "Tensilica Patents Raise Eyebrows").

Numerous forces work in ARM's favor. ARM's grip on mobile phones is still strong, and although phone sales are less spectacular than they were a few years ago, it's still a lucrative growth market that spans the globe. Between 2002 and 2006, the handset market is expected to grow 31%, according to market analysts at In-Stat/MDR. The migration to 2.5G and 3G phones with integrated digital cameras, web browsers, videogames, and other CPU-intensive functions will create more demand for powerful 32-bit processor cores that conserve battery life. A new challenger for this market is Intel's XScale architecture—but XScale has an ARM-compatible core, so either way, ARM can't really lose.

PDAs have a bright future, and ARM-based OMAP chips from Texas Instruments and DragonBall chips from Motorola are powering the next generation of PalmOS products. The ARM-based Gameboy Advance from Nintendo is a hot product, although game-playing mobile phones are slowing sales in Japan. In Europe, ARM benefits from the transitions to 32-bit smartcards and advanced set-top boxes. Long design cycles in the automotive and storage markets help soften the recessionary dips that affect other industries, and ARM enjoys strong positions in both markets. Inkjet printers continue to do well because of their rapidly evolving capabilities and the soaring popularity of digital cameras, and ARM cores are found in many popular printers from Hewlett-Packard and Lexmark. Portable MP3 players are a hit with youngsters, rapidly replacing Walkman-style cassette and CD players; ARM-based Maverick audio chips from Cirrus Logic led the way.

As ARM gains momentum, the ARM architecture attracts even more third-party support in development tools, peripheral IP, and electronic design automation (EDA) software. ARM's AMBA bus for connecting on-chip cores is so widespread that even some competitors are forced to support it. If ARM's victory over PicoTurbo doesn't discourage other companies from cloning the ARM architecture, at least it will make customers think twice before licensing an ARM clone. PicoTurbo's fall was a pointed reminder that IP providers with staying power are a safer bet for costly projects.

ARM isn't resting on its laurels. In 2002, ARM introduced two processor cores we have nominated for *MPR* Analysts' Choice Awards: the **ARM1026EJ-S** and **ARM1136JF-S**. Both signal a new course for ARM. The company has changed its design flow to produce soft implementations of

ARCompact: An Elegant 16/32-Bit ISA

The ARCompact ISA is a 16/32-bit hybrid that retains the essential advantages of a 32-bit RISC architecture. For one thing, there's no need for explicit mode-switching between 16- and 32-bit instructions. Assembly-language programmers and compilers can freely mix both types of instructions in the same code without restrictions. ARCtangent-A5 automatically decodes the different instructions before feeding them into a common pipeline.

As a result, there's no mode-switching penalty in the form of special instructions, and interrupt handlers can use both types of instructions interchangeably—two important distinctions from ARM's Thumb. Furthermore, the 16- and 32-bit ARCompact instructions make preserving memory alignment easier than do Tensilica's 16- and 24-bit instructions.

Another advantage of ARCompact is the way it handles register addressing. Shorter instructions necessarily have fewer bits for encoding register addresses, so they usually can't access the full set of 32 registers considered standard in a 32-bit RISC architecture. Most of the ARCompact 16-bit instructions reserve only three bits each for the source and destination operands, so they can access only eight registers. However, some 16-bit ARCompact instructions reserve three bits for one operand and six bits for the other. This allows them to access the full set of 64 core registers (32 standard registers plus 32 optional extension registers) in the ARCtangent architecture.

Among the 16-bit instructions with extended register addressing are some commonly used operations, such as MOV, CMP, ADD, and SUB. This feature saves memory and improves performance by reducing the need for extra instructions to shuffle data between registers.

In addition to code compression, the ARCompact ISA offers other improvements. It has several new 32-bit instructions, such as a compare-and-branch instruction that does the work of two previous instructions and some bit-manipulation operations of particular value for networking applications. The ARCompact ISA also greatly expands the number of opcode slots available for user-defined custom instructions. Developers can now add as many as 128 16-bit instructions and 128 32-bit instructions, compared with 69 user-defined instructions in the A4 ISA. As before, any of these instructions can support conditional execution based on 16 predefined or 16 user-defined condition codes.

One disadvantage of ARCompact is some additional complexity in the processor's decoder logic, which must scan each instruction header to determine the instruction length. The additional gate delays in this critical path slightly reduce the maximum clock frequency of ARCtangent-A5 in a given fabrication process, compared with that of the A4. The difference is relatively small—perhaps 10%—and is partly or wholly offset by the improved efficiency of the new ISA and the instruction cache. (Shorter instructions effectively increase the size of the cache, so fewer cycles are wasted on cache misses.)

Another drawback of ARCompact is binary incompatibility with code compiled for earlier ARC processors, but migrating to the new ISA isn't difficult. The programmer's models for the two instruction sets are similar. In many cases, developers can simply recompile their high-level source code for ARCompact. In addition, a new switch in ARC's MetaWare High C/C++ compiler automatically generates binary executables that substitute 16-bit instructions for many 32-bit instructions, so hand-coded in-line assembly language isn't required.

new microarchitectures first, followed by optimized hard cores. This policy acknowledges the big gains that soft cores have made in recent years. Although some customers still need the maximum performance that only a custom layout can achieve (given the current limitations of EDA tools), more customers are demanding the greater design flexibility that synthesizable cores can deliver. This trend is also leading toward greater configurability, which ARM hasn't yet fully explored, but the company's new emphasis on soft IP is in step with the market.

The ARM1026EJ-S was an important product in 2002 because it was ARM's first synthesizable ARM10 core. ARM tuned the instruction pipeline for flexible timings and greater compatibility with caches of compiled RAMs. The ARM1026EJ-S also includes Jazelle, ARM's Java-acceleration extensions. In another important development, ARM released certified EEMBC benchmark scores for the closely related ARM1020E variant—the first (and so far, only) ARM core with certified EEMBC scores.

An even bolder new product is the ARM1136JF-S. As the first ARM11 core, soft or hard, it's the debutante of ARM's new design flow, and it introduces significant improvements over previous ARM cores. It has an integrated DMA controller for tightly coupled memories (which are more deterministic than caches), two branch-prediction modes (static and dynamic), and surprisingly high clock-frequency targets for a soft core: 400MHz (worst-case) and 500–700MHz (typical) in a 0.13-micron CMOS process. What makes this possible is an eight-stage instruction pipeline, the longest of any ARM processor.

Among the other improvements in the ARM1136JF-S is an FPU that's truly integrated, not simply bolted onto the coprocessor interface; this should boost floating-point performance and yield more-efficient die layouts. DSP extensions

and 16-bit Thumb instructions are standard; an MMU allows the ARM1136JF-S to run sophisticated embedded operating systems; and the whole thing weighs in at 330,000 gates (excluding caches or tightly coupled memories), quite reasonable for a 32-bit processor with all these features. The first licensees are LSI Logic, Qualcomm, and TI.

Looking forward to 2003, ARM is taking steps to further reduce the power consumption of its processors by working with National Semiconductor on a new voltage/frequency-scaling technology. Like AMD's PowerNow, Intel's SpeedStep, Transmeta's LongRun, and VIA's LongHaul, ARM's technology will regulate the processor's voltage and performance, using software feedback. ARM claims it will improve upon existing techniques by 10–15%, a claim yet to be independently verified.

We also expect ARM to gradually make its synthesizable processors more user-configurable, a path pioneered by ARC and Tensilica and recently followed by MIPS. Although neither ARC nor Tensilica has matched ARM's financial success, their configurable processors (and certified EEMBC scores) prove that a few custom instructions can greatly boost application performance while costing almost nothing in die area and power consumption. Greater configurability would be a logical extension of ARM's embrace of flexible soft IP.

Improv Tackles Media Processing

By far the most unusual contender for the *MPR* Analysts' Choice Award in the IP Core Processor category is the **Jazz DSP** and **Crescendo** "solution kit" from Improv Systems. This is the second generation of Improv's VLIW media-processor core and development software, which designers use to create a custom processor known as a Jazz DSP. Although we chose to exclude DSPs from the IP-core category this year, the Jazz DSP isn't really a digital-signal processor in the traditional sense. It's more accurately described as a customizable media processor with DSP and parallel-processing capabilities. In any case, it differs radically from the general-purpose processor cores that constitute the rest of this category.

Improv's configurable architecture is unique. Designers can combine as many as 16 computation units and five memory controllers, all connected to an integrated bus multiplexer. A proprietary interface known as QBus communicates with other on-chip components, and Improv's solution kit includes bus models for ARM and MIPS coprocessor interfaces and AMBA. In other words, a Jazz DSP core is designed to work in concert with other soft microprocessor cores, not necessarily compete against them.

Consumer electronics are the prime target for Crescendo, especially products that need to run high-performance audio and video codecs. The Crescendo solution kit has software libraries for common media formats (such as MPEG-4, MP3, Dolby Digital, and Windows Video) and even some management code for ARM and MIPS host processors. Additional solution kits include Acappella for voice-over-packet applications and Tempo for home networking products. Improv understands that such an unusual processor architecture is unlikely to attract as much third-party tool support as a general-purpose architecture, so the company strives to offer self-contained support packages.

Certified EEMBC scores show that Improv is a worthy contender. Improv ran the EEMBC telecommunications suite on cycle-accurate simulations of two different Jazz DSP configurations under EEMBC's out-of-the-box and full-fury rules. (Under out-of-the-box rules, Improv compiled the benchmark source code with its C compiler instead of optimizing the code in assembly language, so the exercise was a rigorous test of Improv's development tools as well as of its processor. Under full-fury rules, Improv was allowed to optimize the benchmark code for even better results.)

Although Improv didn't win the highest absolute score for a simulated processor at its target clock speed—that honor belongs to the blazing-fast 2GHz Intrinsity FastMath—the 250MHz Jazz XT did achieve the highest out-of-the-box TeleMark score per clock cycle, evidence of an efficient architecture. Figure 1 shows the out-of-the-box benchmark results.

Figure 2 shows what a Jazz DSP can do with some optimizing. Although the 2GHz FastMath still attained the

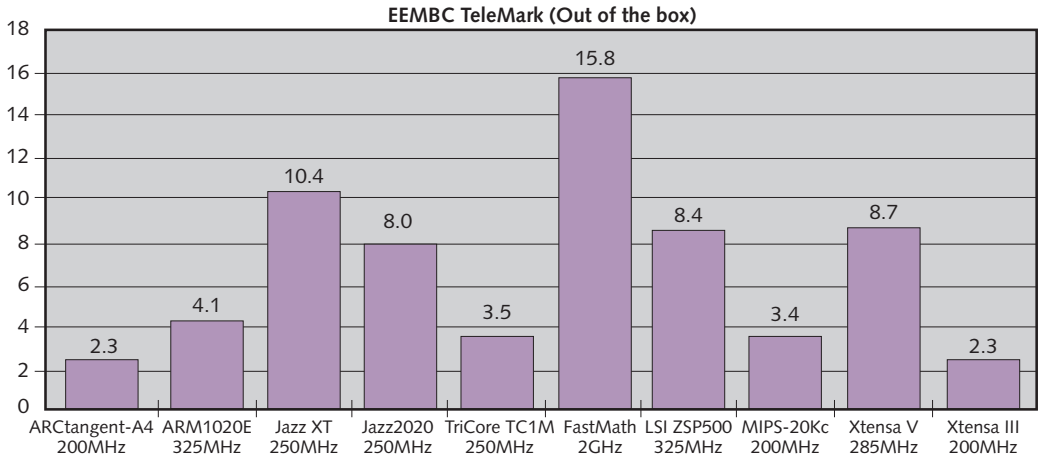

Figure 1. *MPR* scaled the EEMBC TeleMark scores to each processor's target clock speed, based on the cycle-accurate simulator results at 1MHz. Although the Intrinsity FastMath achieved the highest TeleMark, its target frequency of 2GHz is eight times higher than the 250MHz Improv Jazz XT, which finished second. Improv's Jazz2020 and Tensilica's Xtensa V also did well in this test.

highest absolute score at the target clock frequency, the 250MHz Jazz XT isn't far behind. This figure also shows how a few custom instructions can greatly improve performance with other configurable processor cores, such as the ARCtangent-A4 and Tensilica Xtensa III and Xtensa V.

Improv's challenge in 2003 is to sell a high-performance but difficult-to-describe architecture to developers who tend to favor familiar solutions. General-purpose embedded processors—even the soft cores—offer steadily rising performance and are easier to comprehend. With the notable exception of graphics processors in PCs, specialized media processors often have trouble competing against general-purpose architectures.

One development in 2002 that will help Improv reach more customers is its participation in IBM's Blue Logic IP Collaboration Program, an association of IP vendors. As part of the Blue Logic IP library, the Jazz2020 is available to IBM's ASIC customers for a license fee starting at $150,000, depending on the configuration. Four preconfigured Crescendo cores and a preconfigured Acappella core are part of the library.

MIPS Embraces Configurability

The MIPS architecture continues to enjoy widespread popularity in the 32-bit embedded market, generally aiming for higher-performance applications than the lower-power ARM cores. It doesn't hurt that the clean, relatively simple MIPS RISC architecture is a teaching tool at hundreds of universities, so that young engineers and programmers graduate having a familiarity with the architecture. This plants the seeds for future design wins and helps keep MIPS well supported by third-party development tools and software.

At EPF 2002, MIPS introduced the MIPS32 M4K synthesizable microprocessor core, which implements the latest revision of the MIPS32 ISA. The M4K has new features for hardware-supported multitasking, lower interrupt latencies, chip multiprocessing (CMP), bit manipulation, and greater configurability. All these improvements reflect the demand for powerful SoCs in communication, networking, and storage applications. They also justify our nomination of the **M4K** for an *MPR* Analysts' Choice Award in the IP Core Processor category.

Hardware-supported multitasking is a well-timed enhancement; in the PC market, Intel is making a big splash with Hyper-Threading, a similar but more powerful technology. (In 2001, Hyper-Threading won the Analysts' Choice Award for Best Technology.) The MIPS32 implementation gives designers the option of integrating up to four duplicate register files for rapid context switching among as many different tasks. In embedded processors, this kind of multitasking is valuable because it enables low-latency interrupt handling in hard real-time applications. Moreover, it's a configurable option in the M4K, so designers can save gates by implementing only one or two register files.

For multicore SoCs, the M4K has improved interprocessor communication and synchronization, including semaphores to control access to shared memory. Earlier MIPS synthesizable cores didn't allow designers to use the memory-lock signals that make this possible, although some licensees implemented their own protocols. The enhanced MIPS32 ISA also has better debug support for CMP designs.

The most intriguing new development for MIPS in 2002 was a step toward the broad configurability previously offered by ARC and Tensilica exclusively. The M4K and some other MIPS32 cores now permit any designer to add custom instructions to the base MIPS32 ISA, a privilege formerly reserved for MIPS32 architecture licensees, not core licensees. Designers can create as many as 16 new instructions to accelerate application-specific algorithms and critical sections of programs. After designers write the instructions in register-transfer-level (RTL) code, MIPS has provisions for modifying the software-development tools and simulators to recognize the extensions.

MIPS is only now revealing in detail how its configurable design flow works, and it falls short of the mature configurable technology from ARC and Tensilica. However, it provides much more flexibility than was previously available from MIPS or is currently available from ARM. It also validates what ARC and Tensilica have been saying all along: a soft microprocessor core should be a malleable design element, not just a synthesizable translation of a rigid hard core. We expect MIPS to offer even more configurability in the future. The only potential obstacle is legal: new patents by ARC and Tensilica could limit MIPS's maneuvering room.

A significant difference between MIPS and other processor-IP vendors is the MIPS64 ISA: no other company openly licenses 64-bit microprocessor cores. MIPS offers both soft and hard implementations of its 64-bit architecture—the 5Kc and 20K cores, respectively. That gives MIPS an advantage

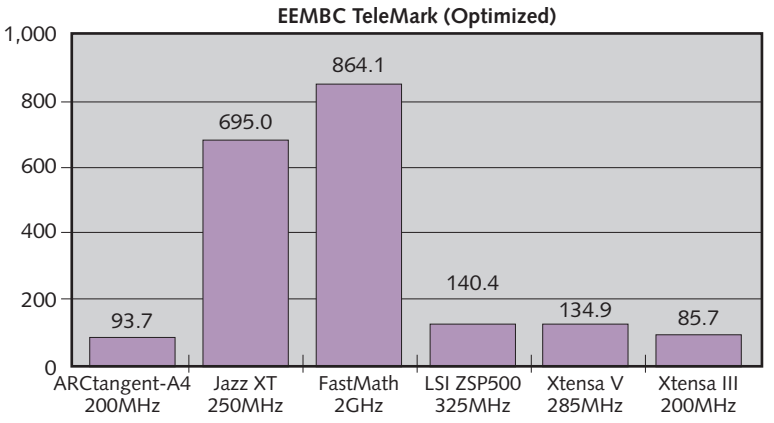

Figure 2. These optimized EEMBC TeleMark scores show spectacular gains over the out-of-the-box scores; compare the numbers with those in Figure 1. *MPR* scaled these scores to each processor's target clock frequency from the cycle-accurate simulator results at 1MHz.

when competing for high-performance designs. We expect MIPS to continue defending this exclusive turf in 2003. New competition might come from IBM, which is rumored to be considering open licensing for the PowerPC architecture.

Tensilica Stays Focused, Pushes Hard

Tensilica was a busy bee in 2002, announcing a new version of its configurable microprocessor core (Xtensa V), new VLIW extensions (FLIX), support for IBM's CoreConnect bus, record-breaking EEMBC benchmark scores, and four important technology patents. The company continued to accumulate licensees and business partners, such as Agilent, Cypress, FujiFilm Microdevices, Hudson Soft, Olympus, OptiX Networks, Trebia Networks, and Xilinx.

Xtensa V isn't a major upgrade over Xtensa IV, but it's definitely worthwhile. With help from custom instructions, a simulated 260MHz configuration of Xtensa V racked up a higher EEMBC ConsumerMark score (optimized) than any other tested microprocessor, smoking even a 1GHz (unoptimized) PowerPC. As Figure 3 shows, only a similarly optimized configuration of the ARCtangent-A4 gave Xtensa V any serious competition. **Xtensa V**'s stellar performance and new features justify our nomination for an *MPR* Analysts' Choice Award in the IP Core Processor category.

Unlike ARC, the company's closest competitor, Tensilica focuses exclusively on configurable processor cores and related tools. Tensilica's catalog has no peripheral IP, system software, middleware, or unrelated products inherited from corporate acquisitions. Depending on one's point of view, that's either good or bad. While it allows Tensilica to concentrate its resources on a single product line, it also means the company must rely on third parties to provide the other embedded IP and software components required to design well-integrated SoCs and top-to-bottom system solutions. As a relatively small, young company, Tensilica lacks the wide industry support enjoyed by longer-toothed competitors like ARM and MIPS.

One of Tensilica's strategies is to cozy up with IBM. In addition to adopting IBM's CoreConnect bus, Tensilica joined IBM's Blue Logic IP Collaboration Program. IBM has qualified the Xtensa core for manufacturing in the IBM Microelectronics 0.13- and 0.18-micron CMOS processes, so IBM's ASIC customers can select Xtensa from a broad portfolio of Blue Logic IP. In fact, Tensilica became the first Platinum member of the program, which indicates that at least one customer has an Xtensa-based design in volume production at IBM.

Likewise, Tensilica joined Xilinx's AllianceCore program in 2002. Among other benefits, Tensilica's new XT2000-X processor-emulation system uses a Xilinx Virtex-II FPGA, which allows developers to customize, synthesize, and begin testing an Xtensa V design in a matter of hours. The Virtex-II system runs 50% faster than previous Tensilica emulation boards, which used Altera FPGAs. (Altera was an early investor in Tensilica.)

In the past, Tensilica has been more aggressive than archcompetitor ARC in pursuing the vital Asia-Pacific market, where most of the world's largest consumer-electronics companies provide fertile soil for IP-core licensing. ARC was more Europe-focused: it was founded in the U.K., employs most of its workers there, and is publicly listed on the London Stock Exchange. That orientation began to change in 2002, when ARC's new CEO established his executive offices in Silicon Valley and began courting more Asia-Pacific customers. Despite this fresh competition, Tensilica still has strong ties in the region, inking deals in 2002 with important customers like FujiFilm, Olympus, and ETRI (Korea's government-supported SoC design center).

Keeping busy didn't insulate Tensilica from the weak technology market last year. Like many companies, it was forced to cut expenses and shed employees. Because it's still privately held, Tensilica's finances are less transparent than those of public companies like ARC, ARM, and MIPS. Had the stock market continued on the ballistic trajectory of the 1990s, Tensilica might have gone public by now, raising a mountain of new capital. But an IPO could be disastrous in today's tech-hostile business climate, even though Tensilica in no way resembles a dot-com. As a result, Tensilica has been forced to survive on current revenues and the money it has raised from private investors: a total of $64 million since the company was founded in 1997, with the last round of $31 million in April 2001. That cash will have to last until Tensilica becomes profitable, raises more private funds, or determines that an IPO is realistic.

Tensilica's strengths are good microprocessor cores, easy-to-use configuration tools, solid business partners, a growing stable of customers, future royalty streams, and technology-savvy managers with a clear vision. A budding patent portfolio doesn't hurt, either, and might deter competitors from imitating Tensilica's technology. However, the stiff

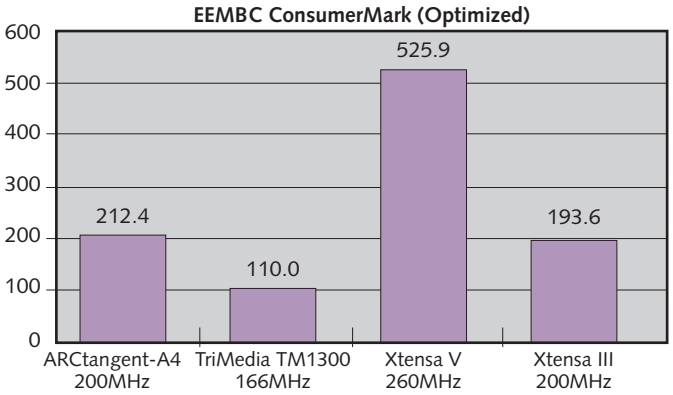

Figure 3. Thanks to custom instructions, Tensilica's Xtensa V processor established a new speed record in the EEMBC consumer suite. All these processors deliver impressive optimized performance, surpassing the unoptimized scores of most other processors by an order of magnitude. In comparison, the fastest unoptimized CPU was Motorola's 1GHz PowerPC MPC7455, which scored a ConsumerMark of 122.6.

competition from ARC, ARM, and MIPS—all publicly traded and well-capitalized companies with similar processors—will continue to be an obstacle for Tensilica in 2003. So will ARC's deep discounts on up-front license fees, which could snatch customers from Tensilica or force it to offer similar discounts.

Analysts' Choice Award: Judging a Winner

We're fortunate to have so many outstanding microprocessors in the IP-core category in 2002, especially after the economic gales of the past two years. We believe that designers who understand the requirements of their applications and take time to explore the capabilities of these processors can't go seriously wrong with any of them. And thanks to the trend toward greater configurability, designers who can't find exactly what they want can create customized processors with potentially stunning application performance.

Still, we have to pick a winner in this highly competitive category, so we choose the **ARM1136JF-S** for the *Microprocessor Report* Analysts' Choice Award for **Best IP Core Processor** of 2002.

We believe the ARM1136JF-S is a significant new processor for both ARM and the industry. For ARM, it's the first ARM11 core—soft or hard—and the most architecturally sophisticated core the company has ever produced. It has Java acceleration, DSP extensions, optional tightly coupled memories, dynamic branch prediction, an MMU, and a fully integrated FPU, making it suitable for a wide range of modern embedded applications. Thanks to a deeper pipeline and attentive design effort, it can reach clock frequencies once considered outlandish for a synthesizable processor. It's a major step forward in the evolution of the ARM architecture. We think the ARM1136JF-S raises the bar for soft cores and will be a hit with designers who need high performance with low power consumption.