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AMD and IBM to Develop Fab Technology

Engineers Will Collaborate On 65nm and 45nm Fabrication Processes

By Tom R. Halfhill {1/27/03-01}

AMD's new alliance with IBM to jointly develop 65nm and 45nm fabrication technology should relieve some pressure on AMD in the race to keep up with Intel. It also raises the possibility that AMD will take the larger step of using IBM as a foundry for chip manufacturing—either instead of or in addition to outfitting its own 65nm and 45nm fabs.

The multiyear deal, in which AMD is paying IBM an undisclosed amount of money, relocates 40–50 AMD engineers to IBM's new 300mm-wafer fab and development center in Fishkill, New York. They will work with IBM engineers to develop 65nm and 45nm fabrication processes, scheduled to debut in 2005 and 2007, respectively. AMD will use the technology to build future versions of its x86-compatible PC and server processors. IBM can use the same technology for PowerPC processors, ASICs, and other chips.

It's a mutually compatible marriage, because both companies need high-performance processors to compete with Intel, yet they compete with each other only marginally. AMD will gain access to IBM's world-class research; IBM gains an experienced development partner and a valuable customer.

Earlier Deal With UMC Looks Shaky

This isn't the first such marriage for AMD. A previous union with Motorola successfully developed copper interconnects and other techniques until it expired last year. However, a recent engagement with UMC might end up with the Taiwanese company stranded at the altar. AMD is breaking off a technology-development alliance with UMC in favor of the IBM relationship, and a deal with UMC to build a new 300mm-wafer 65nm fab in Singapore may be unconsummated, too. The tech downturn has left UMC's existing 300mm-wafer fab in Taiwan with unused capacity, reducing the likelihood that UMC will spend billions on a similar fab elsewhere.

If AMD and UMC don't collaborate on the Singapore fab, AMD will have to build or retool a 65nm fab alone or with another partner; use IBM as a foundry for 65nm production; or do some combination of both. Outfitting a fab takes at least two years, so to begin production in 2005, AMD must decide soon. The decision will come within the next few months, according to Bill Siegle, AMD's chief scientist and senior vice president of technology operations.

Joining forces with IBM—at least for technology development and possibly for foundry services—makes a lot of sense. Both companies want to use silicon-on-insulator (SOI) transistors with strained silicon and 65nm lithography, and IBM has already created operational test chips combining those technologies. (See *MPR 12/30/02-03*, "IBM Adds Strained Silicon to SOI.") It's still early enough in the development phase for AMD and IBM to adapt their respective microprocessor designs to the new fabrication technologies and to align their manufacturing processes. Figure 1 shows AMD's new roadmap.

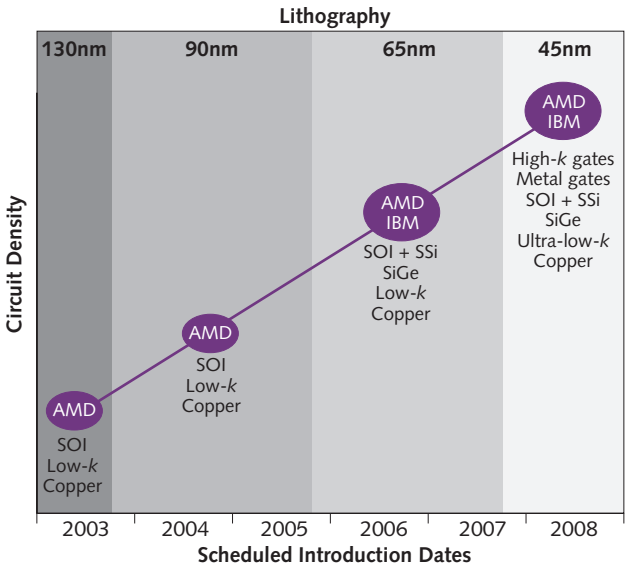

Figure 1. AMD's roadmap anticipates the debut of SOI this quarter, strained silicon (SSi) with SOI and silicon germanium (SiGe) in 2005, and more-advanced technologies in 2007.

They can't afford to delay, because Intel plans to introduce strained silicon on a more aggressive schedule: it will appear in the Prescott version of Pentium 4 when Intel's 90nm process debuts later this year. However, Intel doesn't plan to add SOI until the 65nm generation in 2005. (See *MPR 9/3/02-01*, "Intel Adopts Strained Silicon.") IBM has been using SOI in PowerPC chips since 1999, and AMD plans to introduce it with the Athlon 64 and Opteron x86-64 processors this quarter. AMD's earlier adoption of SOI will roughly counterbalance Intel's earlier adoption of strained silicon. Both technologies can significantly improve a chip's performance and power consumption.

The IBM alliance could supersede AMD's previous relationship with AmberWave Systems to develop strained silicon. AMD has been working with AmberWave to develop strained silicon on bulk CMOS. (See *MPR 4/22/02-01*, "AmberWave Commercializes Strained Silicon.") AmberWave isn't completely out of the picture, but it's clear the development project with IBM will define AMD's technology roadmap.

Intel Plans to Use EUV By 2009

Although AMD and IBM won't say if they'll extend their relationship beyond the 45nm node, AMD will probably find it advantageous to do so. Intel recently announced it will begin mass-producing chips with extreme ultraviolet (EUV) lithography at the 32nm node, scheduled for 2009. (See *MPR 6/19/00-01*, "Extreme Lithography.") In response, IBM said it will introduce EUV at about the same time as Intel. Sharing EUV development with AMD could save money for both companies.

The IBM relationship will have little or no effect on AMD's already developed 90nm process, scheduled to debut later this year. However, the companies will collaborate on a range of advanced technologies for the 45nm generation: high-*k* gate dielectrics, metal gates, and ultralow-*k* dielectric insulators, according to Bijan Davari, vice president for technology and emerging products at IBM Microelectronics. The companies may have to resolve differences between their existing low-*k* insulator technologies for 65nm production, because AMD currently uses chemical vapor deposition (CVD) to spray the insulating film on wafers, whereas IBM uses SiLK, a spin-on dielectric resin from Dow Chemical.

AMD and IBM have collaborated before. When AMD acquired NexGen in 1996, it inherited the almost-finished Nx686 processor, which became the AMD K6. NexGen had designed the Nx686 for IBM's C4 flip-chip packaging because IBM was fabless-NexGen's foundry. Rather than redesign the Nx686 for its own packaging—which would have seriously delayed the processor's debut and probably impaired its performance—AMD licensed C4 from IBM and implemented the technology in its own fabs. Although their new alliance requires a much greater degree of collaboration, it helps to have had a successful working relationship in the past.