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IBM Adds Strained Silicon to SOI

Advanced Fabrication Technology Accelerates Future Transistors

By Tom R. Halfhill {12/30/02-03}

IBM Microelectronics has successfully produced the first short-channel nMOS transistors using silicon germanium (SiGe) and strained silicon with a silicon-on-insulator (SOI) substrate. The test chips, which have thousands of operational transistors, pave the way for IBM to introduce a combination SOI/strained-silicon fabrication process with 65-nanometer (nm) lithography in 2005. The payoff will be higher clock frequencies or lower power consumption, depending on the chip designer's priorities.

Scientists from IBM described their experiments in a paper at the IEEE's International Electron Devices Meeting (IEDM) in San Francisco. Their research yielded two impressive conclusions: a single fabrication process suitable for mass production can successfully combine SOI, SiGe, and strained silicon; and the enhanced electron mobility of strained silicon is sustainable with transistors that have very short gate lengths.

IBM found that even at effective gate lengths (L_{eff}) measuring less than 60nm, strained silicon with SOI can increase current flow through nMOS transistors by nearly 25% over that of identical SOI-only transistors. Previous experiments either used larger transistors or didn't combine strained silicon with SOI. Figure 1 shows a scanning-electron micrograph of IBM's 60nm transistor.

Strained silicon is suddenly hot technology. In August, Intel said it would introduce strained silicon with its next-generation 90nm process in 2H03, two years before IBM. (See *MPR 9/3/02-01*, "Intel Adopts Strained Silicon.") However, Intel doesn't plan to add SOI until the 65nm generation in 2005, about the same time IBM introduces its combination SOI/strained-silicon process at 65nm. AMD is rolling out SOI with its Athlon 64 and Opteron processors in 1H03 and says it will also adopt strained silicon by 2005.

IBM contends it's better to introduce SOI first and add strained silicon later, because SOI is easier to manufacture and yields immediate benefits in performance and power consumption, even without strained silicon. IBM was the

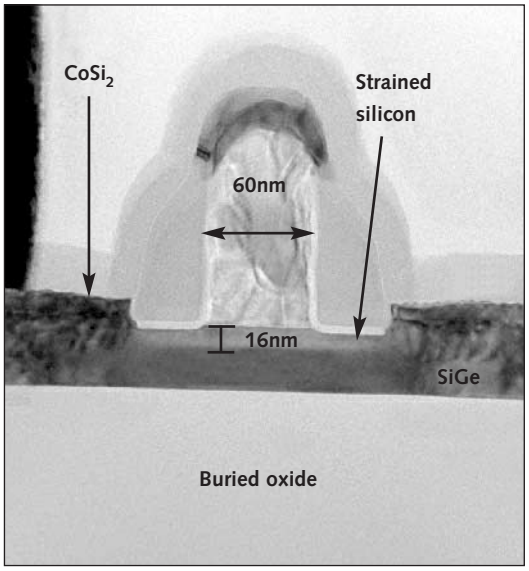

Figure 1. At the base of IBM's experimental transistor are thin layers of strained silicon and silicon germanium on the wafer's silicon oxide substrate. The surrounding cobalt disilicide ($CoSi_2$) on the raised source/drain layer reduces source-to-drain resistance.

For More Information

Conference proceedings of the 2002 IEEE Electron Devices Meeting (ISBN 0-7803-7463-0) are available from the IEEE Online Catalog & Store at *http://shop.ieee.org/store/*. Price is $125 for IEEE members or $250 for nonmembers.

first company to put SOI into mass production: SOI first appeared with the 0.22-micron (220nm) CMOS-7S process in 1999 and is a common feature in IBM's PowerPC chips.

Secret Sauce: Thin SiGe

There are different ways to implement strained silicon. Intel and AMD haven't disclosed their processes in detail. A strained-silicon pioneer, AmberWave, has experimented with adding graded layers of SiGe to bulk silicon wafers, followed by a silicon cap layer. (See *MPR 4/22/02-01*, "AmberWave Commercializes Strained Silicon" and *MPR 4/29/02-02*, "Strained Silicon, Part 2: Applications and Future Directions.") However, IBM says any manufacturing technique that adds relatively thick layers of SiGe to the wafer is time consuming, can increase current leakage from the transistors, and can cause more defects.

Instead, IBM deposits thin layers of SiGe (about 35nm total) on the silicon oxide substrate, capped by a thinner silicon layer (about 16nm thick). The "relaxed" atomic structure of the SiGe stretches the silicon atoms in the tightly bonded cap layer further apart (by about 1%), allowing electrons to flow more freely through the silicon. Result: faster transistors. Or, by using the technique with larger transistors or lower voltages, designers can reduce static-current leakage and save power.

Combining strained silicon with SOI creates a process that IBM calls SGOI (silicon germanium on insulator). IBM says the advantages of SGOI are higher drive currents, lower capacitance, fewer defects, and easier manufacturing. Using an experimental 60nm (L_{eff}) SGOI nMOS transistor, researchers measured an improvement in AC efficiency of 22% over that of a 55nm SOI-only nMOS transistor. The improvement is less dramatic with pMOS transistors, so the actual speed boost for a mass-production CMOS device will be less than 22%, but it's still worthwhile.

SGOI also lays the foundation for future advances in process technology, such as high-*k* gate dielectrics, which can reduce a transistor's static-current leakage by a factor of 1,000. Because a high-*k* gate insulator tends to reduce electron mobility, combining this technique with strained silicon maintains, or even improves, the speed of the transistors. In June 2002, IBM announced the first field-effect transistor (FET) made with strained silicon and high-*k* gate dielectrics.

Intel's surprise announcement about introducing strained silicon in 2003 miffed IBM, even though the companies don't compete to provide foundry services. (With a few exceptions, such as some PA-RISC chips formerly manufactured for Hewlett-Packard, Intel's fabs are almost entirely dedicated to in-house chip production.) IBM considers itself—with justification—the world leader in cutting-edge process technology and is jealous of interlopers. The IEDM paper builds the case that it's worth waiting two years for a strained-silicon process combined with mature SOI. It also ups the ante by disclosing more technical details, assuring customers that IBM is still on track with its technology roadmap. ◇