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INTEL SPILLS THE BEANS ABOUT BANIAS

New Mobile CPU and Chip Set Have Numerous Power-Saving Features

By Tom R. Halfhill {11/25/02-01}

Intel has disclosed intriguing details about its future Banias mobile processor at recent industry conferences, including **Microprocessor Forum 2002**. In addition to describing some of the chip's power-saving techniques, Intel emphasizes that Banias is a comprehensive "mobile platform," not just a lower-power CPU. At launch in 1H03, the platform will include mobile processors at various speed grades, two core-logic system chip sets, and dual-band 802.11a/b wireless networking.

Intel is pursuing several long-term goals with Banias. First, to extend the battery life of mobile computers to eight hours or more; second, to increase mobility by making wireless networking a standard feature; third, to maintain a high level of CPU performance within the thermal limits of mobile systems; fourth, to encourage the evolution of new mobile products, such as tablet PCs.

Unless Intel springs a last-minute surprise, Banias won't introduce any revolutionary new technology that dramatically slashes power consumption. There will be no radical architectural makeover, as Transmeta engineered with its VLIW-based Crusoe processors and hardware-assisted software emulation. (See *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier.") Instead, Banias processors conserve power in many little ways: by reducing static and dynamic power consumption at the circuit level; by improving execution efficiency at the microarchitectural level; by providing finer control over the core voltage and frequency at the CPU level; and by saving bus power at the chip I/O level.

At its core, Banias is a hybrid of a shorter-pipelined, Pentium III–style design with a Pentium 4–style front-side bus (400MHz) and SSE2 extensions. Within these boundaries, the Banias team doggedly worked to conserve every possible watt. At times, the team traded off tiny percentages of performance to save tiny percentages of power. These efforts may be less dramatic than Transmeta's clean-slate approach, but it's the results that matter. By steering a more conservative course, Intel will almost certainly find a better balance between the longer battery life and high performance users demand.

Although Intel hasn't publicly disclosed the power specifications for Banias, a recent statement contains a clue. Several new tablet PCs will use the ultralow-voltage (ULV) mobile Pentium III-M processor, which Intel says was the first PC processor to operate at less than 1V while consuming less than 0.5W (average). According to Intel, Banias processors will "further improve" on those specifications in second-generation tablet PCs. Of course, "average power" is difficult to quantify in the absence of industry-standard benchmarks. A thermal design power (TDP) comparison would be more informative, because it specifies the power envelope system designers need to know, but Intel hasn't released those numbers yet.

Initially, the main market for Banias will be laptop PCs, with smaller numbers of the processors going into tablet PCs and high-density blade servers. Not by coincidence, laptops constitute the only segment of the PC market with a healthy pulse. While desktop PC sales and profits remain flat, the combined annual growth rate of unit sales in the mobile PC market is 15%. Average selling prices are higher, too, so mobile PCs are generally more profitable. Therefore, Intel's Banias

disclosures are most interesting for what they reveal about the company's future mobile strategy.

Technology Trends Make Banias Inevitable

Intel didn't announce it was working on a new low-power x86 design until after Transmeta's much-hyped coming-out party in February 2000. That led to the widespread conclusion that Banias was a competitive response to Transmeta. However, that conclusion was mistaken, according to Mooly Eden, general manager of Intel's Israel Design Center, headquarters of the Banias team. Eden insists the Banias project was under way before Transmeta announced its Crusoe processors. Of course, Intel's upper management may have had an inkling of Transmeta's plans and reacted by conceiving the Banias project. Whatever the case, Eden's assertion is plausible.

ROSS MEHAN

Mooly Eden, general manager of Intel's Israel Design Center, unveils new details about Banias's power-saving techniques at MPF 2002.

For years, chip designers have been wrestling with the power dilemma of deep-submicron fabrication processes. Although smaller processes enable lower core voltages, which reduce power consumption, the denser chips must dissipate more heat from a smaller area, and static current leakage from inactive transistors becomes a relatively greater problem. At geometries of 90 nanometers (nm) and smaller, the transistors' gate oxides are so thin that quantum effects like electron tunneling may become significant. As they go forward, CPU architects will have to make more trade-offs between power consumption and performance.

Unfortunately, Intel missed a major opportunity when it decided, a few years ago, to let IBM, AMD, and Motorola take the lead with silicon-on-insulator (SOI) transistors. SOI reduces transistor-junction capacitance by as much as 50%, which enables a higher clock frequency at a given power level or lower power at a given clock frequency. (See *MPR 08/24/98-02*, "SOI to Rescue Moore's Law.") PowerPC processors have been using SOI since 1998, and AMD plans to introduce SOI in its x86-64 processors in 1Q03. It's not on Intel's roadmap until 2005.

Intel is no doubt looking at other techniques to reduce power at the process-technology level, but the company's flexibility is limited by its longstanding strategy of standardizing its fabs and manufacturing mobile CPUs in the same basic process as high-performance desktop and server CPUs. Any technique at the process level that reduces power consumption at the expense of performance would probably be unacceptable, because it would make Intel's desktop and server CPUs less competitive. So far, Intel hasn't announced plans to alter its process-technology strategy by manufacturing mobile CPUs in a specialized process.

Instead, Intel is taking an alternate route to low power with Banias: specialization at the circuit, microarchitecture, and system levels. Banias is evidence that the designs of desktop and mobile CPUs are diverging more than ever before. The historical practice of retargeting slightly modified desktop processors for the mobile market is reaching a limit. Just the fact that Intel moved the responsibility for designing Banias to an independent team in Israel is a sign of the new priorities. Until now, Intel assigned the work of "mobilizing" CPUs to a secondary team that started with a hand-me-down design from the desktop team.

If the only way CPU vendors can remain competitive is to create special microarchitectures for each market segment, Intel will be in a strong position. Intel is one of the few companies with enough resources to design and maintain separate desktop and mobile microarchitectures. It will be difficult for AMD to follow suit—and almost impossible for any other x86 vendor. Furthermore, Intel's leadership in system chip sets and PC system architecture makes it easier for the company to tackle the power-consumption problem at multiple levels, not just in the CPU. And indeed, that's what Intel is doing with Banias.

Intel Looks Beyond the CPU

The first Banias processor will be accompanied by two new north-bridge chips, code-named Odem and Montara-GM. Their main difference is that Odem has an AGP-4x graphics interface, and Montara-GM has integrated graphics with no option for upgraded graphics. Montara-GM also has two digital-video output ports and an integrated LCD interface with low-voltage differential signaling (LVDS). Both chips support DDR SDRAM and have a 400MHz CPU interface (100MHz base clock frequency with four data phases per clock period).

Together, the CPU, system chip set, and graphics chips consume about 30% of the power in a mobile PC, so Intel's reason for trying to practice holistic medicine is apparent. But the other big power sinks are the backlit LCD and the mechanical disk drives, which are beyond Intel's direct control. To influence the evolution of those components, Intel annually publishes a "Mobile Platform Vision Guide" and participates in an industry consortium known as the Extended Battery Life Working Group. Both initiatives seek new ways to conserve energy and stretch battery life.

Another vital part of the Banias platform is wireless connectivity. This feature hasn't made it into the core logic yet, but the first Banias laptops will have a dual-band 802.11a/b Wi-Fi radio (code-named Calexico) on a mini-PCI card, to be followed shortly by wireless integration on the motherboard. Eventually, Intel will reduce its 802.11 solution to a single chip. (See *MPR 10/7/02-01*, "Intel Shows Standards Solidarity.")

Although wireless connectivity may seem peripheral to the goal of reducing CPU power consumption, it's actually

an important facet of Intel's mobile strategy. Eden describes a symbiotic relationship: wireless integration will create more demand for longer battery life as users get accustomed to anywhere-anytime Internet access, so making wireless a must-have feature will drive more customers toward Banias. Wireless integration will also drive down costs and probably establish Intel's solution as the de facto industry standard. That, in turn, should lower the cost barriers and reduce the interoperability hassles that slow the widespread adoption of wireless connectivity.

Finally, Intel sees new classes of mobile computers emerging and doesn't want to surrender that ground to other low-power x86 vendors like Transmeta and VIA. Banias is designed to work within the stricter thermal limits of tablet PCs as well as with full-size laptops, notebooks, and subnotebooks. Although Banias processors won't satisfy the even-lower power requirements of PocketPC- and Palm-class handheld computers, Intel can pursue that market with its ARM-based StrongARM and XScale chips. In sum, Banias is a key part of a coherent mobile strategy.

No Magic Bullet

If there's a magic bullet for cutting power consumption, Intel hasn't found it yet. It's evident from Intel's disclosures that the Banias team has tackled the problem at every possible level—from the gate lengths of individual transistors to the voltage and frequency ranges of the microprocessor.

As Eden explained at Microprocessor Forum, the Banias engineers evaluated every design element by balancing the relationships among performance, power consumption, and battery life. A key concept is that battery life represents a fixed amount of energy available to a mobile system. The CPU can perform a finite number of calculations on a battery charge, so there's an energy penalty for using more clock cycles, sometimes even when the additional cycles contribute to higher performance. With AC power, the trade-offs are different, because the amount of energy available is essentially infinite. The CPU dissipates wasted clock cycles as heat, which is a cooling issue but not an energy-capacity issue.

Among the first elements that attracted the attention of the Banias team was the on-chip L2 cache. This cache would be unnecessary if memory latencies weren't lagging so far behind CPU speeds, and the huge SRAM arrays sometimes occupy half the die. The first Banias processors will have a 1MB L2 cache—twice as large as the L2 caches in existing mobile Pentium 4-M processors. Of the 77 million transistors in a Banias CPU, we calculate more than 50 million are in the L2 cache. While it's true that SRAM arrays consume relatively less power than active logic circuits, a cache that accounts for two-thirds of the transistors in a processor is something to be reckoned with.

Intel's first step was to divide the eight-way set-associative cache into four power domains per way. That yields 32 domains, each 32K in size. The chip can shut off power to domains that aren't being accessed and rapidly switch them on when an associated tag indicates a hit in a domain. (To shorten a critical path, the tag-decoder logic runs down the center of the cache.) At any moment, the chip must power only 1/32 of the cache memory, plus the decoder logic and tags. Eden says this totals about 3–4% of the L2 cache circuitry; the rest of the transistors can sleep.

To minimize static current leakage from the cache logic, Intel modified some of the NAND gates and optimized the gate lengths of the transistors. Normally, the output of a NAND gate is high if one or both inputs are low, and the output is low if both inputs are high. When a modified NAND gate isn't in a computational mode and needs to supply a high output, the processor steers both inputs low instead of leaving one input high. Of course, the truth table remains the same, as Table 1 shows. Although the modified NAND gates complicate the design of the cache logic, Eden says the static current leakage drops by a factor of five.

To further reduce static leakage, Intel defined a minimum gate length (L_{eff}) for all transistors in the logic surrounding the cache, such as the tag decoders. Normally, some of the transistors might have shorter gates, causing more leakage. Holding all transistors to a minimum gate length reduced that leakage (and also slightly cut their active power consumption).

Unfortunately, this caused another problem: the longer-gate transistors switch more slowly, and distributing them throughout the cache logic created a critical path that was unable to meet the timing target of the CPU. Consequently, accessing the L2 cache takes one extra clock cycle. Such a compromise would probably be unacceptable in a desktop processor—and certainly in a server processor. It's acceptable in Banias because, according to Eden, it reduces power consumption by more than 1W.

This example—and the more extensive clock gating that Intel has implemented throughout the processor—is indicative of the fine detail work and small power/performance trade-offs wrought by the Banias design team.

Triple Branch Prediction Saves Cycles

Another example of the way Banias delicately balances power and performance is the processor's sophisticated three-level dynamic branch predictor. The objective was to reduce the number of clock cycles wasted on instructions the processor must flush from its pipelines and caches when an unexpected branch changes the program flow. Wasted clock cycles impair both performance and energy conservation.

Input		Output	Comments
0	0	1	Very low leakage; both N-channel transistors off
0	1	1	Some leakage; V_{cc} drop across only one transistor
1	0	1	Some leakage; V_{cc} drop across only one transistor
1	1	0	No leakage; both P-channel transistors off

Table 1. Intel modified some NAND gates in the cache logic to reduce static current leakage.

Banias has three branch predictors that use different methods to predict various kinds of branches. The first or "bimodal" predictor is for branches that almost always jump in the same direction, such as tests for exceptional error conditions. The second or "local" predictor bases its guesses on the dynamic history of a particular branch; this is like the original Pentium's branch predictor, which assigned a 2-bit history value to each branch (weakly taken, strongly taken, weakly not taken, strongly not taken). The third or "global" predictor bases its guesses on the pattern of recent branches executed before the current branch, not necessarily on the branch itself. Intel's P6 processors (Pentium Pro, Pentium II, and Pentium III) used this method. As Figure 1 shows, Banias can mux the outputs of all three predictors to make a forecast.

Eden says the triple branch predictor in Banias reduces wrong guesses by more than 20%, according to simulations. He estimates the improved branch predictor will boost performance by 5% and reduce power consumption by 3%, even with the added prediction logic.

Not enough details are known about Pentium III and Pentium 4 branch predictors to make a detailed comparison with Banias. Pentium III has a two-level predictor that's probably 90–95% accurate, judging from the benchmark results of two-level predictors in other types of processors. If Banias makes 20% fewer mispredictions than a two-level predictor, it's probably at least 95% accurate. Intel says Pentium 4 does even better when compared with Pentium III, improving the prediction rate by about 33%. Pentium 4 is known to have a larger branch target buffer than Pentium III (4KB vs. 512 bytes) and a better prediction algorithm. However, Pentium 4 probably works differently than Banias, because it has an L1 trace cache instead of a conventional instruction cache. The trace cache stores decoded micro-ops for the predicted execution path, avoiding micro-ops jumped by branches.

Another target for Eden's power misers was the input buffers on the system bus. When a CPU issues a read instruction that misses the on-chip caches, it must wait for the data to arrive over the bus from memory. While it's waiting, a Banias CPU can switch off its input buffers to save power. Meanwhile, the north-bridge chip snoops the bus. Two clock cycles before the data is ready, the north bridge signals the CPU to activate the input buffers, effectively hiding the latency of awakening them. To further optimize these operations, Intel says Banias will also have some new and improved prefetch instructions.

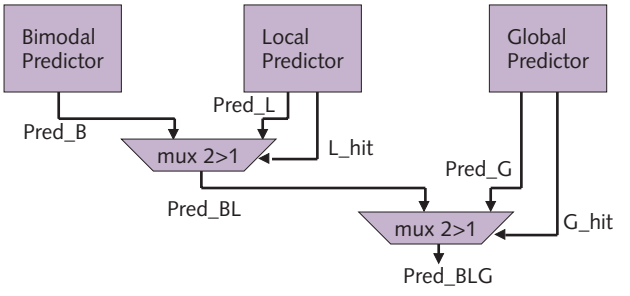

Figure 1. The three-level branch predictor in Banias improves on the two-level dynamic branch prediction in Pentium III processors, which is believed to be the starting point for the Banias design. Intel hasn't disclosed the sizes of the branch target buffers.

Although Intel hasn't estimated the amount of power all these bus-management techniques will save—obviously, it greatly depends on the application—they will probably add up to a few percent, like the other small economies in Banias.

Making a Jigsaw Puzzle of Micro-Ops

One curious feature of Banias is what Intel calls "micro-op fusion." Banias will join some pairs of micro-op instructions into a single instruction that remains intact as it flows through the rest of the pipeline. In some cases, the fused pairs will be split up again during the execution stages.

What's curious about micro-op fusion is that it reverses the process that created the micro-ops in the first place—and then, in some cases, reverses it again.

Micro-ops exist to simplify the CISC instructions of the x86 architecture. The x86 has variable-length instructions (they can range from 8 bits to 120 bits long) that often combine multiple operations, such as arithmetic operations and direct memory references. For instance, a single instruction might load an operand from memory, add it to another operand from a register or memory, and store the result to memory. These complex instructions are more difficult to decode, schedule, and execute, especially in a superscalar processor that executes instructions out of their original program order. The common work-around in almost all x86 processors since Pentium II and AMD K5 is to decode the CISC instructions into simpler RISC-like micro-ops that execute arithmetic and logical operations in a register-to-register fashion and that segregate memory references as load/store instructions.

Micro-op fusion reverses the fission and puts some of the split instructions back together again. And, in some cases, a fused pair of micro-ops undergoes a second fission.

Unfortunately, Intel hasn't disclosed details of these transformations or provided any examples. We assume micro-op fusion doesn't wholly restore an original x86 instruction; otherwise, all that expensively engineered decoder logic could be bypassed with a wire. More likely, Banias fuses pairs of sequential arithmetic/logical instructions that operate on register operands without external memory references. For the cases in which Banias splits the fused pair again, perhaps the sequential instructions are free of mutual data dependencies, so the CPU can execute them in parallel. We'll have to wait until Intel releases more details to fully understand this process.

However, the purpose of micro-op fusion is clear. By pairing some micro-ops and handling them as a single instruction, Banias can increase its instructions-per-cycle (IPC) ratio. That saves power by doing more work in fewer clock cycles.

Another unsolved mystery is the dedicated stack manager briefly described at the Intel Developer Forum. Apparently, Intel has added some new logic to better manage the stack pointers and other accounting busywork inside the processor. Like micro-op fusion, it's supposed to reduce the propagation of micro-ops. One possibility is that it eliminates (or executes earlier) some operations that explicitly manipulate the stack. Again, anything that pares down the number of micro-ops will increase the IPC and save power.

The most recent company to announce an x86 processor is also promising to make stack operations more efficient. MemoryLogix says its new MLX1, a synthesizable x86 core for SoCs, has special logic to accelerate some types of load and pop operations. (See *MPR 11/11/02-02*, "MemoryLogix Makes Tiny x86.") Perhaps Intel is doing something similar with Banias.

A Speedier SpeedStep?

Banias will introduce the third version of SpeedStep, Intel's dynamic voltage/frequency scaling. SpeedStep could have a much greater effect than any of the aforementioned techniques, because the power consumption of a microprocessor varies linearly with the core frequency but quadratically with the core voltage. Transmeta was the first x86 vendor to exploit this equation in a new way by introducing LongRun technology with the Crusoe TM5400 processor in 2000. (See *MPR 7/10/00-02*, "Top PC Vendors Adopt Crusoe" and the sidebar, "Transmeta Explains LongRun.") LongRun monitors the operating system to dynamically scale the core voltage and frequency in response to software demands.

Since then, other x86 vendors have introduced similar features: AMD has PowerNow, VIA has LongHaul, and Intel has SpeedStep. One advantage of LongRun is that it works at a lower level than the operating system, because it's part of Transmeta's code-morphing software—the x86 emulation layer that runs on the inner VLIW processor core. The other methods work at the operating system level and aren't invisible to the system.

The first version of SpeedStep, officially unveiled the day before Transmeta's announcement in 2000, was relatively primitive: it simply reduced the core voltage and frequency when a mobile PC was unplugged from AC power, then restored the normal levels when the computer was reconnected. (See *MPR 1/17/00-05*, "PC Processor Competition Consolidates.") In 2001, Intel introduced Enhanced SpeedStep. It still has only two voltage/frequency levels, but the levels can vary under dynamic software control with either AC or battery power. (See *MPR 8/6/01-01*, "Intel Debuts 1.13GHz Tualatin.") Banias will have Advanced Enhanced SpeedStep, a further refinement of the technology.

Intel says the new SpeedStep allows much finer software control over the core voltage and frequency; exactly how fine hasn't been disclosed. Transmeta's LongRun is capable of 32 steps, though in practice it needs only about a half-dozen to be effective. When asked during a discussion panel at Microprocessor Forum to explain the difference between the new SpeedStep and LongRun, Eden said Intel's technology can hold the CPU's I/O voltage steady to achieve a wider range of variable core voltages. But LongRun also does that.

Another difference Intel cites is the linkage between core voltage and frequency. The new SpeedStep has a unique voltage for every frequency, whereas LongRun has multiple frequency steps for each voltage level.

Sources have told *MPR* about a potentially more-important difference: the new SpeedStep can change the processor's voltage and frequency more quickly than LongRun can. According to these sources, Banias doesn't have to stop and restart the CPU clock, even when adjusting voltage and frequency over very wide ranges. If this is true, it would be an improvement over LongRun, which must stop the clock, change the frequency, change the voltage, wait for the voltage to stabilize, wait for the PLL to lock onto the new frequency, and then restart the clock. Execution stalls while the clock is stopped, of course.

Transmeta says the worst-case latency for a LongRun voltage/frequency swing is 20 microseconds and almost never more than 10 microseconds. That's fast enough to make adjustments while decoding sequential MPEG-2 frames in a DVD movie. If Intel has found a way to eliminate even that small latency while avoiding the transient problems of clock skew and voltage instability, a Banias processor running at gigahertz speeds could execute several thousand instructions in the few microseconds it takes a Crusoe processor to switch gears.

One thing to consider is the way a faster SpeedStep would avoid disrupting the operating system and application software while throttling the processor. Some programs are sensitive to a sudden clock-speed adjustment. By briefly stopping the CPU clock, LongRun can soften the shock.

Furthermore, LongRun's subterranean home below the operating system means it need not invoke an operating system-level interrupt to make an adjustment. If the new SpeedStep works at a higher level than LongRun does, it may have to trigger an operating system interrupt that takes longer to handle. Keep in mind that operating systems like Windows and Linux aren't designed for hard real-time operations; a heavyweight interrupt handler could slog through several thousand instructions, erasing any time saved by not stopping the clock.

We can do little more than speculate about Advanced Enhanced SpeedStep at this point. It appears, however, that Intel has improved the technology, and that Banias will offer greater voltage/frequency flexibility than existing Intel mobile processors do.

Banias Performance Will Complicate Marketing

Banias-based laptops are months away from reaching stores, but already they have provoked a minor controversy at industry conferences and in the usual Internet newsgroups. Early demonstrations of Banias prototypes indicate they will deliver more raw performance than their clock frequencies

imply. That means Intel will have to veer from its customary marketing strategy of directly linking clock speeds with performance.

Of course, it's not surprising that a CPU with a different microarchitecture has a different relationship between clock speed and performance. This is particularly true when comparing the shorter-pipelined Banias with the superpipelined Pentium 4. Banias was designed for low power consumption with acceptable performance; Pentium 4 was designed for high clock frequencies and high performance, with relatively little regard for power consumption. On some tasks, a Banias processor could deliver almost the same performance as a Pentium 4 running at roughly twice the clock speed.

This will force Intel's marketing department to promote Banias with a figure of merit based on benchmark scores, not clock frequencies. At the same time, Intel's desktop/server marketing will (presumably) continue to promote clock frequencies.

Publicly at least, Intel claims it doesn't see a problem. Intel says its marketing has always emphasized actual performance, not just clock speeds. However, there's no denying the two concepts have become firmly linked in user's minds. Intel's marketing challenge is to sever that link—at least when promoting Banias.

Naturally, this has provoked much merriment and derision among Intel's critics. Intel will now join AMD and Apple in explaining to users why clock speed is not an absolute measure of performance. It appears to be an about-face that validates what AMD and Apple have been saying about their processors all along.

Not exactly, protests Intel. For one thing, Intel says, it won't obfuscate the clock frequencies of Banias processors, as AMD subtly does with the Athlon XP. Although AMD will disclose clock speeds when asked, it prefers to advertise the chip's "model number," which is a pseudo-clock-speed comparison with an Intel processor. For instance, the Athlon XP 2800+ actually runs at 2.25GHz, but its performance is supposed to compare with that of a 2.8GHz Pentium 4. (Benchmark scores are split on this question.) We expect Intel to be more candid than AMD about clock frequencies and to market Banias with a yet-to-be-disclosed performance measurement based on benchmarks.

This isn't the first time Intel has faced the problem of expressing CPU performance in a more abstract way. In 1992, Intel introduced the iCOMP index, a performance rating based on a combination of industry benchmarks. (See MPR 10/7/92, "Intel Unveils 'iCOMP' Performance Index.") Then, as now, the objective was to avoid clock-speed confusion; Intel needed to show that a 33MHz 486 was significantly faster than a 33MHz 386. Intel revised iCOMP in 1996 after introducing the first Pentium with MMX extensions. (See *MPR 07/08/96-02*, "Intel Updates Its iCOMP Index.") However, neither users nor the press ever embraced iCOMP, and it needed frequent revisions to keep pace with new CPU designs. Intel quietly dropped it after a few years.

It's not clear how Intel would avoid a similar fate with a Banias performance index. Ideally, all CPU vendors would agree on a performance-rating system that allows fair comparisons among different PC processors, much as EEMBC has done for embedded processors. Unfortunately, that goal seems as remote—and nearly as difficult to negotiate—as lasting peace in the Middle East.

The Quest for All-Day Mobile Computing

Banias is a significant departure for Intel. Although Intel's mobile processors have incorporated many power-saving enhancements over the years, at heart they've always been desktop processors designed for maximum performance, not low power consumption. Historically, a new desktop microarchitecture went mobile when a process shrink reduced power to tolerable levels. That strategy leveraged a single microarchitecture across multiple markets, but it caused a delay of 12–18 months before the next process shrink made the new design practical for mobile PCs. The strategy didn't put Intel at a disadvantage, because other x86 vendors did the same.

Everything changed in 2000, when Transmeta introduced the first line of x86-compatible processors especially designed for low power. (There is some debate about this; some believe Transmeta initially aimed for high performance, but its x86 emulation fell so far short of the target that the company resorted to a low-power strategy.) Transmeta originally promised "all-day computing," much as Intel is now striving for eight-hour battery life with Banias. However, Transmeta's promise remains unfulfilled. Crusoe-based subnotebooks can't run all day on a battery charge—though some run for six hours, considerably better than the usual two to four hours most users expect from a laptop.

Despite introducing an innovative microprocessor design for a fast-growing mobile market, Transmeta has found success elusive. Intel continues to dominate, trailed at a distance by AMD. Transmeta's share is lost in the noise of the "other" category in market-research pie charts.

One of Transmeta's problems, of course, is that Intel is a formidable competitor. Every design win is an uphill battle. Another problem is that mobile users are reluctant to compromise performance or features to get longer battery life. They vote with their dollars for faster CPUs, bigger LCDs, larger-capacity hard drives, more memory, and movie-capable DVD-ROMs. Perhaps one reason is that many people use mobile PCs as transportables rather than true portables, moving their systems from one AC-connected site to another. In addition, more people seem to be adopting mobile PCs as their only PC, so they're even less willing to sacrifice desktop features and performance.

All that could change if Intel's bet on wireless pays off. If untethered network access becomes ubiquitous, and mobile PCs are free to roam, users may recognize their wall wart and power cord for what they are: a ball and chain. Suddenly, battery life will be fashionable.

Whether the Banias project was purely a reaction to Transmeta or a proactive assault on the dilemma of power consumption is academic. What's important is that it was necessary. To maintain its leadership position, Intel is compelled by physics to design different microarchitectures for desktop and mobile PCs, just as it's doing for servers. One size no longer fits all. Even if Banias fails for some reason, Intel will have to try again. Indeed, as process geometries continue to shrink, Intel will have to keep trying harder; there's no turning back.

One cause for concern—based on what's known so far—is that Banias doesn't introduce any breakthrough power-saving technology. To trim a few watts here and there, Intel is fiddling with transistors, NAND gates, micro-ops, and branch predictors. Although the Banias engineers deserve credit for their hard work, some of their efforts seem like a strenuous climb for high-hanging fruit. That's usually a sign that a mature technology has no more surprises to be discovered, no more opportunities for improvement by leaps and bounds. And that bodes ill for future chips made in even smaller submicron processes. The power-consumption vise keeps tightening.

Ultimately, pursuing the goal of all-day mobile computing inside the microprocessor may prove futile. Every contribution helps, but the larger part of the solution lies elsewhere. If the CPU, core logic, and graphics chips account for 30% of the power consumption in a mobile PC, then eliminating them altogether would extend three hours of battery life to only four hours. To reach eight hours, mobile PCs will almost certainly need lower-power displays, more-efficient disk drives, and new battery technologies—innovations that will come from other companies, not from Intel.

Price & Availability

Intel will begin shipping Banias processors and chip sets in 1H03. No prices or speed grades have been announced.