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IBM PowerPC 405EP Expands Family

SoC Targets Wireless LANs, Edge Routers, Broadband Modems

By Tom R. Halfhill {11/11/02-03}

IBM is sampling the PowerPC 405EP, the newest member of its popular 405 family of SoCs. Among other features, the 405EP adds a second 10–100Mb/s Ethernet controller for greater flexibility in small routers and wireless LAN access points. The 405EP is also intended for DSL/cable modems and other network-edge products.

The new chip is based on the 405D4 embedded processor core, an evolution of the 405B3 core introduced with the first chip in this series, the 405GP (see *MPR 7/12/99-03*, "PowerPC 405GP Has CoreConnect Bus"). It's a 32-bit CPU core with 16K instruction and data caches, an MMU, a 64-entry TLB, four timers, and a JTAG debug interface. IBM wraps various combinations of on-chip peripherals and interfaces around these cores to create several different SoCs for low-cost networking applications. A 64-bit version of IBM's CoreConnect on-chip bus ties the CPU core and peripherals together.

Notable additions to the 405EP are the second Ethernet MAC, five general-purpose timers, and eight more general-purpose I/O pins (32 in the 405EP vs. 24 in the 405GP). Notable subtractions are CodePack decompression, the 32-bit peripheral bus, external bus mastering, and support for synchronous PCI. Furthermore, the 405EP supports only three external PCI masters, vs. six in the 405GP. Table 1 shows the differences among the 405EP, 405GP, and 405GPr chips.

The most surprising difference is the missing CodePack decompression unit. The 405GP was the first processor to support IBM's scheme for decompressing executable code at run time (see *MPR 10/26/98-05*, "PowerPC Adopts Code Compression"). CodePack squeezes code by an average of 40% and seems like a

	PowerPC 405EP	PowerPC 405GP	PowerPC 405GPr
PowerPC core	405D4	405B3	405D4
Core frequency	133/200/266MHz	200/266MHz	266/333/400MHz
SDRAM bus	100/133MHz	100/133MHz	133MHz
L1 cache (I/D)	16K/16K	16K/8K	16K/16K
CodePack	No	Yes	Yes
Peripheral bus	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits
External bus master	No	Yes	Yes
PCI interface	Asynchronous	Sync/Async	Sync/Async
PCI external masters	3	6	6
Ethernet MACs	2	1	1
Timers (core + chip)	4 + 5	4	4
GP I/O pins	Up to 32	Up to 24	Up to 24
Dhrystone MIPS	404 @ 266MHz	404 @ 266MHz	607 @ 400MHz
Voltage (core, I/O)	1.8V, 3.3V/5V	2.5V, 3.3V/5V	1.8V, 3.3V/5V
Power (est. typical)	1.0W @ 200MHz	1.5W @ 200MHz	1.1W @ 266MHz
IC process	0.18µm Cu CMOS	0.25µm Al CMOS	0.18µm Cu CMOS
Package sizes (enhanced PBGA)	31 x 31mm	25 x 25mm 27 x 27mm 35 x 35mm	27 x 27mm 35 x 35mm
Pin count	385	413, 456	456
Availability	Nov-02	Now	Now
Price (10K)	$17 @ 133MHz	$24 @ 200MHz	$30 @ 266MHz

Table 1. The new PowerPC 405EP is designed for lower-cost networking applications. It has fewer features and pins than the most closely related 405-series chips, although it does add some goodies, such as a second Ethernet MAC.

Price & Availability

The PowerPC 405EP is sampling now. IBM plans to begin production in November. Prices are $17 for 133MHz, $22 for 200MHz, and $27 for 266MHz in 10,000-unit quantities. For more information, visit *www.ibm.com/chips*.

useful feature in an embedded processor. However, IBM says it dropped CodePack from the 405EP because few customers use it. Apparently, SDRAM is so cheap and plentiful that memory conservation is less important than it used to be.

By chopping the 32-bit peripheral bus down to 16 bits and removing some capabilities from the PCI controller, IBM managed to reduce the 405EP's pin count, even with the addition of the second Ethernet MAC and extra GPIOs. (The SDRAM bus is still 32 bits wide.) IBM says the narrower peripheral bus will have little real effect on performance, because most peripherals in the products for which the 405EP is intended have 16-bit interfaces.

The 405EP will be fabricated in IBM's SA-27E CMOS process, a 0.18-micron process with 0.13-micron effective gate lengths (L_{eff}) and copper interconnects. In contrast, the 405GP is still fabricated in IBM's older SA-12E process, a 0.25-micron process (0.18-micron L_{eff}) with aluminum interconnects. Instead of using the process shrink and higher-conductivity metal layers to boost clock frequencies, IBM is offering the 405EP at the same speed grades as the 405GP and reaping the benefits in power consumption. The new chip consumes about 50% less power than the 405GP at the same clock rate.

In addition, the 405EP costs a few dollars less than the 405GP. It's a good deal for customers who don't need CodePack or 32-bit peripherals and could put the second Ethernet MAC to good use. Although IBM markets the 405-series chips primarily for networking applications, the only significant feature that sets them apart from general-purpose processors is the Ethernet integration. Actually, they are suitable for a variety of embedded systems.

Not surprisingly, the relatively minor differences between the 405EP and 405GP aren't reflected in IBM's estimates of their Dhrystone 2.1 benchmark scores: both deliver 404 mips at 266MHz. EEMBC benchmark scores might be more illuminating, but they aren't publicly available yet and probably never will be, if IBM follows the pattern established with the 405GP. Although IBM has obtained certified EEMBC results for that processor, the company has decided against making the scores public, choosing instead to disclose them, under an NDA, to prospective customers only.