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VIA KEEPS IT SIMPLE

C5XL Processor Finally Gets SSE, Faster FPU on Smaller Die

By Tom R. Halfhill {11/11/02-01}

Alone among desktop CPU vendors, VIA Technologies continues to introduce x86 chips unpolluted by superscalar pipelines, out-of-order execution, whiplash-inducing clock speeds, and other frivolous features. Instead, VIA focuses on simplicity, low power consumption, and low cost. At least, that's the gospel according to Glenn Henry, the outspoken president of VIA's Centaur microprocessor division.

Henry described VIA's new C5XL processor and updated his product roadmap at the recent **Microprocessor Forum 2002** in San Jose. True to form, the C5XL shuns the complex features that warm the hearts of power users and the heatsinks of competing chips. Indeed, the C5XL appears to achieve the impossible: it adds a deeper pipeline, Intel-compatible SSE extensions, a faster FPU, support for two-way multiprocessing, a more-efficient L2 cache, and other improvements while actually *shrinking* its size in the same fabrication process. Somehow, Henry's engineers found room for 32% more transistors on a 7% smaller die.

The C5XL is a further extension of the original microarchitecture that Centaur introduced in 1997, before VIA acquired it. (See *MPR 6/2/97*, "Centaur Gallops Into x86 Market.") Many C5XL features were promised at past Microprocessor Forums but hadn't arrived until now (see *MPR 10/23/00-01*, "VIA Still Bullish on Centaur," and *MPR 10/22/01-02*, "VIA Previews C5X Core"). Henry says the C5XL finally taped out last spring, is in wafer production now, and will ship in 1Q03.

In the meantime, VIA has been shipping the C5A, C5B, C5C, and C5N processors. All are plug-compatible with Socket 370, a Pentium III–era interface. Their clock frequencies climbed from 500MHz in 2000 to 1.1GHz today as they migrated from a 0.18-micron process with aluminum interconnects to a 0.13-micron process with copper wiring. Front-side bus frequencies have climbed from 66MHz to 100–133MHz. Along the way, VIA added its own flavor of software-controlled voltage/frequency power management, called LongHaul. Some lower-power derivatives of the C5x family, known as the Eden series, dissipate so little heat that designers have used them in fanless PCs and set-top boxes.

Realistically, nothing is likely to boost VIA's U.S. market share into double digits against the strong competition from Intel and AMD. In Asia, and especially in China, Taiwan-based VIA has better prospects. But even a small share of the worldwide PC-processor market can be lucrative—and VIA is also looking beyond that stagnant market.

Henry says VIA already sells a "substantial fraction" of its x86 processors into embedded systems, such as set-top boxes, Internet appliances, and automotive electronics. He says VIA's embedded sales are growing faster than its PC sales, and that the company's total sales of x86 processors have grown during the two-year-old tech recession. By keeping costs down and hewing more closely to its roadmap, VIA should be able to continue expanding its small niche.

C5XL: Another Evolutionary Step

Although Henry annually preaches against the evils of clock-frequency mania, the C5XL does aim for (relatively) higher

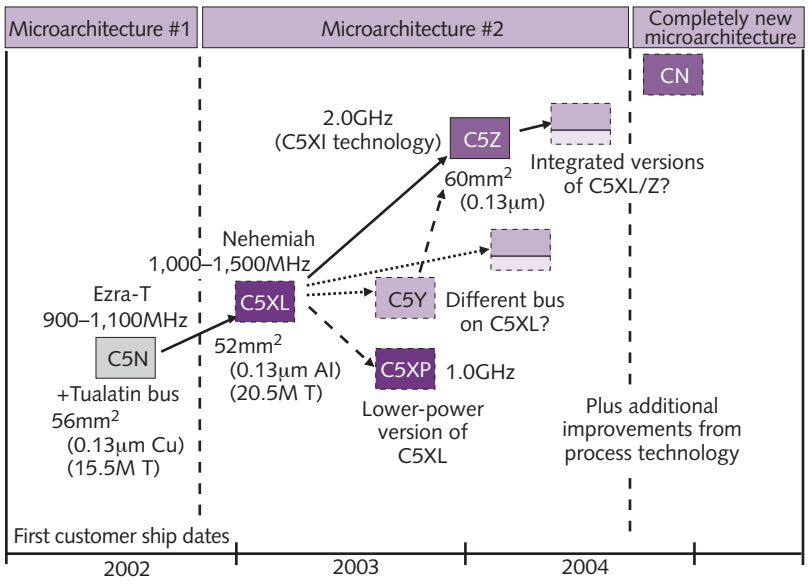

Figure 1. VIA's processor roadmap continues to push the five-year-old Centaur microarchitecture into late 2004, when it may be succeeded by an all-new design. SSE2 is still at least a year away.

speeds: 1.4GHz to 1.5GHz. That's about 50% faster than VIA's current-model C5N processor. To get there, VIA lengthened the basic pipeline from 11 stages to 16. The longer pipeline is more prone to waste clock cycles after a taken branch, so the C5XL compensates with a 1K-entry branch target address cache (BTAC), with each entry identifying two branches. The BTAC works in parallel with fetches from the 64K instruction cache and VIA's unusual branch predictor (see *MPR 12/7/98-05*, "WinChip 4 Thumbs Nose at ILP").

The C5XL's new SSE instructions are welcome, but, in this regard, VIA still lags about two years behind the evolution of the x86 architecture. VIA doesn't anticipate supporting SSE2 until the C5Z debuts in late 2003 or early 2004. The dilemma for VIA is that SSE2 supports dual double-precision floating-point math: a single instruction can operate on two 64-bit floating-point values in a 128-bit-wide SSE register, which would add lots of unwanted silicon to VIA's svelte chips.

Faced with the same dilemma, AMD postponed the hit by supporting most SSE2 instructions in the Athlon XP's 3DNow Professional extensions, but without the dual double-precision math. AMD plans to fully support SSE2 in its 64-bit Hammer-series processors early next year. By the time VIA gets around to supporting SSE2—with or without the dual double-precision math—we expect Intel to have introduced SSE3 in the Prescott version of the Pentium 4. SSE3 will probably add new instructions to accelerate cryptographic algorithms and MPEG4.

Meanwhile, VIA has removed the support for AMD's 3DNow extensions in the C5XL to make room for SSE. This is a sensible trade-off, because virtually all programs that use 3DNow are also compatible with SSE. Figure 1 shows VIA's roadmap for SSE2 and other features in Centaur-family processors.

To fix another weakness, VIA has significantly improved the C5XL's scalar (non-SSE) floating-point performance by clocking the FPU at the full speed of the CPU core. The x87-compatible FPUs in existing Centaur processors run at only half the core frequency. The slow FPUs were a deliberate trade-off, because floating-point performance isn't critical for VIA's target market, and repipelining the FPUs to keep up with the faster cores would have diverted engineering resources from more-pressing needs. The C5XL's FPUs now have longer pipelines and run at the full core frequency.

However, the longer pipelines are more susceptible to unpredicted branches and bubbles; therefore, even though the FPUs are running twice as fast, the performance improvement is less than 100%. According to VIA's tests with the Quake 3 Demo and 3D WinMark 2000 benchmarks—which are more floating-point intensive than most other benchmarks—the C5XL is about 10–22% faster than the C5N at the same clock speed.

	VIA C5XL	VIA C5N
Core frequency	1.0–1.5GHz	900MHz–1.1GHz
Bus frequency	100–133MHz	100–133MHz
Pinout	Socket 370	Socket 370
L1 Cache (I/D)	64K/64K	64K/64K
L2 Cache	64K 16-way	64K 4-way
BTAC	1K entries	None
Vector units	MMX/SSE	MMX/3DNow
APIC for SMP	Yes	No
LongHaul	Yes	Yes
x87 FPU	Full-clocked	Half-clocked
IC process	0.13µm Cu	0.13µm Cu
Transistors	20.5 million	15.5 million
Die size	52mm2	56mm2
Power (TDP)	12–15W @ 1.0GHz	10–12W @ 1.0GHz
Availability	1Q03	Now
Price (1K)	$45 @ 1.0GHz	$42 @ 1.0GHz

Table 1. The C5XL is an evolutionary upgrade over the C5N. Note the removal of 3DNow extensions and the addition of an advanced programmable interrupt controller (APIC) to support two-way symmetric multiprocessing (SMP).

Price & Availability

VIA plans to ship the C5XL processor in 1Q03. The 1.0GHz part will cost $45 in 1,000-unit quantities. For more information, visit *www.via.com.tw/en/index/index.jsp*.

Henry's engineering team made several more enhancements to the C5XL. The 64K on-chip L2 cache is now 16-way set-associative instead of 4-way, which should reduce cache misses by a few percent. The multiplier is a little faster; there's no longer a pipeline penalty for address generation; and return-from-subroutine instructions execute in one cycle. In sum, according to Henry, the C5XL delivers 10–30% more performance than the C5N at the same clock frequency. Table 1 summarizes the differences between the C5XL and the C5N.

To back up his performance claims, Henry showed several benchmark results comparing a 1.0GHz C5XL to a C5N and a Pentium III–class Celeron running at the same frequency, plus a Pentium 4–class Celeron running at 1.7GHz. He normalized all scores to 1.0× for the Pentium III Celeron. Figures 2 and 3 show the results.

ROSS MEHAN

Glenn Henry, president of VIA's Centaur division, presents the C5XL at MPF 2002.

Henry devoted the last section of his Microprocessor Forum presentation to explaining the C5x family's Alternate Instruction Set (AIS). This is a subset of internal micro-ops and registers that are not part of the standard x86 architecture and are normally invisible to programmers. All modern x86 processors from Intel, AMD, and VIA have decoders that break the standard x86 instructions into RISC-like micro-ops for efficient execution. The difference is that VIA allows programmers to write code for the internal instruction set by wrapping the micro-ops in x86 instruction headers—if they know the secret.

Of course, AIS serves no purpose for programmers writing industry-standard x86 software. VIA has been using AIS to write test and debug utilities for internal use only. Recently, the company began revealing the secrets to customers and "qualified users" under an NDA. VIA thinks AIS can be useful to embedded-system programmers whose programs might benefit from the extra registers and RISC-like simplicity of AIS. VIA won't openly disclose the secrets because AIS bypasses some x86 protection mechanisms and could be exploited by malicious hackers.

Henry says two VIA customers are using AIS today. Their code runs on any x86 processor, but when it detects a C5x-family processor, it uses some AIS features to improve performance.

AIS is yet another interesting quirk in a renegade microprocessor designed by a contrarian engineer. Fortunately, the C5XL's other strengths give it enough reasons to exist, and it's likely to continue finding success by flying under Intel's radar.

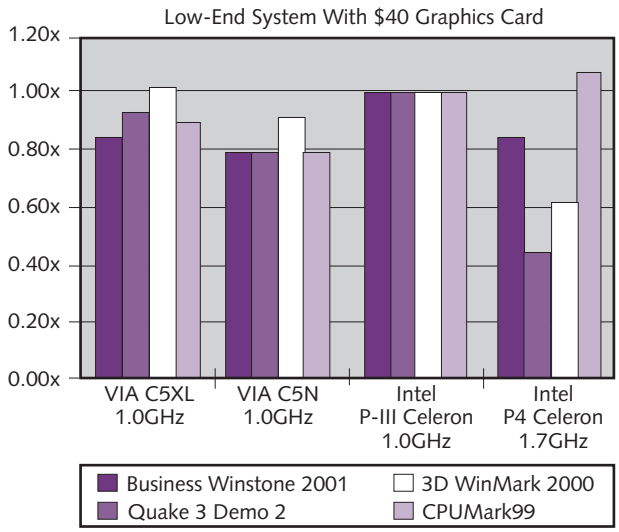

Figure 2. The VIA C5XL compares favorably with two of Intel's value-priced PC processors in a system with a low-end graphics card, according to VIA's benchmark tests. VIA considers the Business Winstone 2001 benchmark the most representative test for the C5XL's intended market.

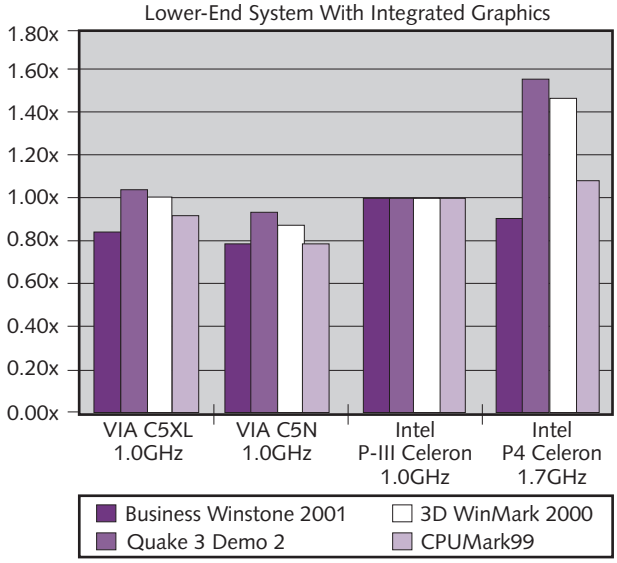

Figure 3. In a lower-end PC with integrated graphics, the VIA C5XL holds it own against a Pentium III–family Celeron at the same clock speed and a Pentium 4–family Celeron running 70% faster, according to VIA's Business Winstone tests. As expected, the superior floating-point performance of the Pentium 4 Celeron is apparent in the Quake 3 and 3D WinMark tests.