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TI Links ARM in OMAP5910

ARM925 and 'C55x DSP Cores Entwined in Standard-Product Chip

By Max Baron and Tom R. Halfhill {9/23/02-01}

Once available to only a few favored customers, Texas Instruments' dual-processor OMAP family is now represented by a standard product. (These days, TI rarely spells out OMAP, which stands for Open Multimedia Applications Platform.) The new OMAP5910 chip unites a slightly modified ARM9TDMI microprocessor core with a TMS320C55x DSP core plus a generous amount of on-chip memory and a host of useful peripherals.

TI is offering the OMAP5910 for embedded applications that need real-time control processing and data-intensive signal processing. Examples might include vertical-market PDAs, biometrics, telematics, car audio systems, and medical equipment. TI has privately supplied previous OMAP incarnations—the OMAP310, OMAP710, and OMAP1510—to Hewlett-Packard, NEC, Nokia, and Palm for 2.5G/3G wireless phones and wireless-communicator PDAs. TI also offers similar, though less powerful, dual-core chips that unite an ARM7TDMI with a 'C54x DSP (see *MPR 1/7/2002-01*, "ARM Shakes Hands With DSP").

All OMAP processors have a similar architecture, although TI has not released the specifications of the private chips. They are believed to have an ARM7- or ARM9-series CPU core, a 'C54x or 'C55x DSP core, various amounts of on-chip memory, different lineups of integrated peripherals, and different clock speeds. The new OMAP5910 has a similar feature set that TI hopes will appeal to a broader spectrum of developers.

Two Cores Use Only 0.25 Watt

The OMAP5910 clocks both the ARM and DSP cores at 150MHz. That's a little slower than the fastest version of the OMAP1510, which drives the ARM core at 175MHz and the DSP core at 200MHz. (Some OMAP1510 chips for private customers run at slower speeds.) TI says it tuned the new chip for a wider range of embedded applications, especially battery-powered products that need lower power consumption. According to TI, despite having two 150MHz processor cores, the OMAP5910 consumed only 230mW in a test that ran an RTOS on each core, exercised the on-chip peripherals, and implemented a GSM full-rate vocoder.

The company has slightly enhanced the ARM9 core and refers to it as the ARM925T or TI925T. Although TI didn't change the instruction-set architecture (ISA), the data and program MMUs now employ a more efficient algorithm than does the off-the-shelf ARM9. In addition, new debug-emulation features allow programmers to debug both the ARM and DSP cores in a single environment with TI's Code Composer Studio, a popular DSP development tool. Otherwise, the ARM925T is a standard 32-bit ARM9. It has a 16K instruction cache, an 8K data cache, two 64-entry TLBs, and 16-bit Thumb instructions.

The 'C55x DSP core offers no surprises, either. It's a 16-bit fixed-point DSP with dual multipliers and ALUs that can execute two instructions per cycle, including two multiply-accumulates (MAC). It has a 24KB instruction cache, 64KB (32K x 16 bits) of dual-access SRAM for data, 96KB (48K x 16 bits) of single-access SRAM for instructions, 32KB (16K x 16 bits) of ROM, and hardware accelerators for DCT, iDCT, pixel interpolation, and motion estimation. The 'C55x is TI's first DSP core to meet the performance and power-consumption requirements of 3G mobile phones; two years

Price & Availability

The OMAP5910 is currently sampling; volume production is scheduled for 1Q03. The price is $32 in 10,000-unit quantities. For more information, visit *www.ti.com*.

ago it won *MPR*'s Analyst Choice Award for Best DSP (see *MPR 1/22/01-05*, "DSPs Give Mixed Signals in 2000").

Each processor core in the OMAP5910 has three private 32-bit timers, a watchdog timer, and its own two-level interrupt handler. The cores communicate over a 32-bit internal bus through four bidirectional mailboxes, sharing 192K of on-chip SRAM and two 16-bit interfaces for external SDRAM and flash memory. The DSP accesses the shared memory via a traffic-controller unit in response to commands from the ARM core.

There are many on-chip peripherals: a nine-channel system DMA controller, a USB 1.1 host/device interface, one USB host/device transceiver, an LCD controller, a Multimedia Card/SecureDigital interface, a camera interface for CMOS sensors, a keyboard interface, a real-time clock, an I^2C master/slave interface, eight serial ports, three UARTs, and up to 14 shared general-purpose I/O pins.

Figure 1 is a simplified block diagram of the OMAP5910. TI is manufacturing the chip in its own 0.13-micron CMOS process. The core voltage is 1.6V, and the I/O interfaces operate at 1.8V, 2.75V, or 3.3V. It's packaged in a 12mm x 12mm 289-ball MicroStar BGA.

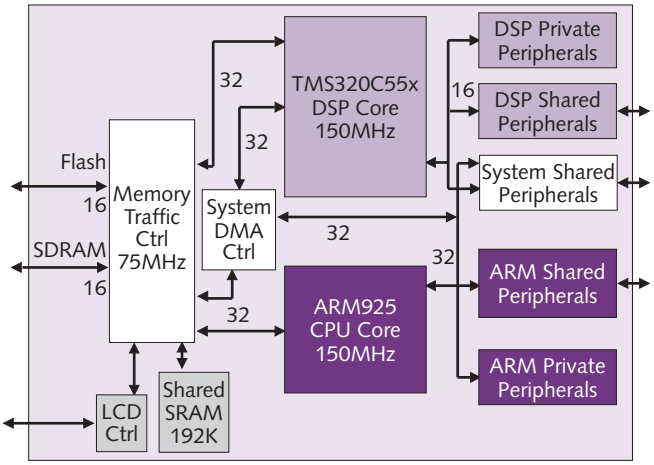

Figure 1. Note the traffic controller (left) that helps manage the memory shared by the ARM and DSP cores. The chip's peripherals are too numerous to diagram (see text). Some system designs may use two identical OMAP5910 chips: one for applications and multimedia and the other dedicated to communications.

Why the Lower Frequency?

Some debate exists about the OMAP5910's reduced frequency compared with that of the fastest version of the earlier OMAP1510. Perhaps TI wants to obtain higher yields for the first OMAP chip that's a standard catalog product, resulting in a more conservative clock-frequency specification. TI has an excellent track record with its 0.13-micron process, so manufacturing limitations probably aren't a factor. Another possibility is that the lower clock rate (and a tardy introduction that follows OMAP's debut by about two years) is the result of business agreements among TI, private OMAP customers, and the owners of intellectual property that contributed to the chip's creation.

Then again, TI's strategy for the 'C55 family tends to favor power consumption over clock frequency, promoting battery life over raw performance. (In contrast, TI's strategy for the 'C64 DSP family emphasizes high performance.) Low power makes sense for a chip like the OMAP5910 that's intended for hand-held mobile products.

If some system designers feel slighted by the lower clock speed and delayed introduction, one compensation is that software support and development tools are more mature than would be expected for a dual-processor chip that's virtually new in the market. Other OMAP developers have presumably uncovered the worst bugs by now. The OMAP family runs a cornucopia of operating systems, among them Linux, Nucleus, Palm OS, Symbian OS, VxWorks, and Windows CE (3.0 and.NET). OMAP also supports TI's DSP/BIOS Bridge, an abstraction layer that lets programmers write the CPU and DSP code in an integrated tool environment. A high-level API calls DSP libraries available from TI, OS vendors, and third parties; the DSP/BIOS Bridge makes the task of writing DSP code less onerous.

TI's superb tools and stable 'C55x instruction set—coupled with the popular ARM9 core—should make the OMAP5910 competitive in the market. Of course, it doesn't hurt that ARM-based processors are already pervasive in the OMAP5910's target market (see *MPR 8/5/2002-01*, "The Long ARM of the Laws of the Industry").

A strong competitor is Intel's XScale PXA250, also designed for PDAs and mobile embedded systems. The PXA250 lacks a DSP core but runs at 200-, 300-, or 400MHz; at the high end, that's more than twice the clock rate of the OMAP5910. The PXA250 is comparably rich in on-chip peripherals: USB (albeit client-only), an SDRAM controller, a flash-memory interface, a color LCD controller, 16-channel DMA, a Multimedia Card/SecureDigital interface, I^2C, I^2S, and other goodies. Deciding which chip has the better peripheral set depends on the application. The PXA250 has no on-chip memory, however (except for a small 2KB cache for streaming data), and it will suffer from the lack of a dedicated DSP when running signal-processing tasks. Power consumption at comparable clock frequencies should be roughly the same, because the PXA250 typically dissipates 500mW at 400MHz, which implies 250mW at 200MHz even without lowering the voltage. Pricing is $19 (200MHz) to $39 (400MHz) for the PXA250 versus $32 for the OMAP5910.

Wireless communicators and PDAs are poised on the edge of huge volumes as 3G technology materializes and low-power microprocessors gain the ability to handle complex video and 3D-graphics processing. The new, broader markets have attracted powerful competitors: AMD, Intel, Motorola, NEC—and now TI.