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Two New MIPS Cores From LSI Logic

By Tom R. Halfhill {7/24/00-06}

LSI Logic is introducing a pair of new MIPS-compatible microprocessor cores for ASICs: the MiniRISC EZ4021 and the TinyRISC EZ4103. Both cores are available now in LSI's EasyMacro format—a physical implementation of the synthesizable models that includes a cache controller, MMU, bus-interface unit, EJTAG debugging, and other features.

The MiniRISC EZ4021 is the more powerful of the two cores. It's based on the 64-bit MIPS-III architecture with multiply-accumulate (MAC) instruction extensions. It runs at 250MHz (worst case) at 1.8V in LSI's G12P process (0.18-micron, four-layer-metal). That's a respectable clock frequency for a synthesized core with a five-stage pipeline. With 16K instruction and data caches, the EZ4021 EasyMacro occupies about 12mm^2 of die area and consumes 650mW (worst case). Performance at 250MHz is about 275 Dhrystone 2.1 mips.

By 2H01, LSI expects to port the EZ4021 to its new 0.13-micron Gflex process, which could boost the clock frequency to 333MHz. It would also shrink the EasyMacro's die area to 3–4mm^2. LSI is developing an enhanced version of the EZ4021 that will add an FPU, MIPS-16 code compression, and configurable caches (16K or 32K each for instructions and data). That core is scheduled for release in 1Q01.

LSI is aiming the MiniRISC EZ4021 at higher-end embedded applications, such as laser printers, scanners, copiers, networking equipment, and midrange set-top boxes. In terms of performance and power consumption, the EZ4021 is comparable to 32- and 64-bit licensable cores and embedded CPUs from MIPS Technologies, IDT, QED, and Lexra.

The TinyRISC EZ4103 addresses a lower end of the embedded market. It's based on the 32-bit MIPS-II architecture and is comparable to an ARM7 core—even including a similar three-stage pipeline. It has MIPS-16 code compression (see *MPR 10/28/96-10*, "LSI's TinyRISC Core Shrinks Code Size"), MAC instructions, EJTAG debugging, and configurable caches (with LSI's cache compiler). In the same G12P

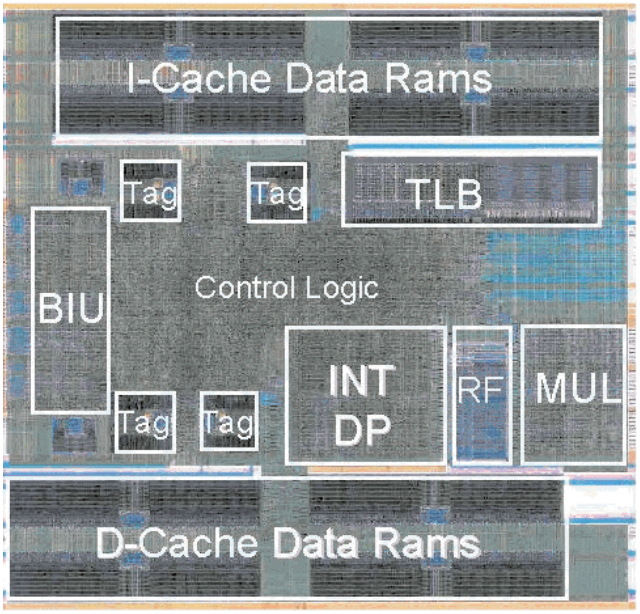

Figure 1. LSI Logic's EasyMacro format is a physical implementation of a synthesizable model, already ported to one of the company's IC processes for easier ASIC integration. This photo shows the MiniRISC EZ4021 EasyMacro in LSI's 0.18-micron G12P process. The macro measures about 3.5mm on each side.

process described above, the EZ4103 runs at 120MHz (worst case) at 1.8V. The EasyMacro occupies 1.9mm^2 of die area in that process, and it consumes only 60mW (worst case, excluding caches). Performance at 120MHz is about 100 Dhrystone 2.1 mips.

LSI is targeting the 32-bit TinyRISC EZ4103 at lower-end and battery-powered embedded applications, such as ink-jet printers, entry-level set-top boxes, storage devices, and miscellaneous consumer electronics. Its stiffest competition will probably come from ARM, not from other MIPS-compatible cores, because the ARM7 comes closer to matching the EZ4103's Lilliputian size and power consumption.

ARM cores and other MIPS-compatible or MIPS-like cores are broadly licensed, allowing customers to port the cores to a foundry of their choice. In contrast, LSI licenses cores for manufacture only in its own fabs. Although LSI's licensing model is less flexible, the EasyMacro can save time and engineering costs and provide more peace of mind for customers worried about botching an ASIC project. LSI also offers extensive technical support and a large library of intellectual property for ASIC integration, which few core vendors can match. The new TinyRISC and MiniRISC cores are valuable additions to LSI's product line, and TinyRISC should be a particularly good ARM wrestler.