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HP AND ST COLLABORATE ON VLIW

By Tom R. Halfhill {1/24/00-03}

Hewlett-Packard Labs and STMicroelectronics have jointly developed a new customizable VLIW embedded-processor technology that will debut later this year. The technology allows developers to rapidly create application-specific VLIW processors with compatible development tools, simulators, and RTOS kernels.

HP and ST embarked on the project in 1997 with the goal of bringing the high instruction-level parallelism (ILP) of VLIW to embedded processors. By itself, that's not a unique idea. In the past year, new embedded VLIW architectures have been announced by Sun (see *MPR 8/23/99-03*, "Sun Reveals Secrets of 'Magic'") and Fujitsu (see *MPR 8/2/99-04*, "Fujitsu FR-V Architecture Bets on VLIW"). High-performance DSPs from Analog Devices, StarCore, and Texas Instruments use VLIW too. And the ability to customize a core for specific applications is the main selling point of ARC Cores and Tensilica, which allow customers to reconfigure and extend their basic RISC cores (see *MPR 5/31/99-04*, "ARC Expands DSP Capabilities," and *MPR 3/8/99-02*, "Tensilica CPU Bends to Designers' Will"). What sets the HP/ST project apart is that it brings developer-driven configurability to a high-performance VLIW architecture for the first time.

In concept, it seems simple. Starting with a basic architecture, embedded-system developers can create application-specific instructions to speed critical routines and algorithms, and they can vary the number of function units and registers in the core. Using automated tools, HP and ST generate a CPU simulator that allows developers to test and refine their custom architecture. This phase might require several iterations. When the performance is satisfactory, HP and ST generate a processor core that meets the customer's specifications, stripping away unneeded instructions and other features that would inflate the die size and waste power. Finally, HP and ST use automated tools to generate a compiler, assembler, linker, debugger, and RTOS kernel that's compatible with the custom architecture.

Furthermore, HP and ST claim that developers can design successive generations of a new architecture while maintaining software compatibility. A weakness of early VLIW architectures was that software often broke on later designs. HP and ST say their technology preserves a common programming model for all members of a processor family—without sacrificing the high ILP of VLIW.

A key component of the technology is a set of highly automated tools that allows HP and ST to quickly crank out the custom architectures and software-development tools with minimal handiwork by engineers. According to HP and ST, the process isn't quite to the point where a single push button does it all, but they believe it's efficient enough to service as many customers as the two partners can sign up.

If the technology works as advertised, the resulting chips could replace DSPs and ASICs in many embedded applications while cutting engineering costs and development time. HP and ST plan to make the technology generally available for evaluation in 2H00, with ST producing and selling the first chips. HP isn't disclosing its product plans at this time, although it's likely that HP will design chips for its own printers, scanners, digital cameras, and other embedded-product lines.

The HP/ST technology will be competition for all licensable cores and especially for embedded ASICs designed around RISC and DSP cores. It also challenges the

configurable-core technology offered by ARC Cores and Tensilica. Both of those companies allow embedded developers to create new instructions and make numerous modifications to proprietary RISC cores.

There are some important differences, however. One is that ARC Cores and Tensilica encourage the development of product-specific chips, while HP and ST intend to develop application-specific processor families. HP and ST say their customization process is still too costly to use to design a special chip for every product. Instead, they intend to create families of processors for categories of products, such as wireless phones or disk-drive controllers. Developers will modify and extend the processors in those families rather than create entirely new chips for similar products.

Another difference is that ARC Cores and Tensilica offer customers the option of manipulating a synthesizable Verilog/VHDL model (or, in the case of Tensilica, a subset of the model). From what is known of the HP/ST technology, developers can add new instructions and specify some other modifications, but HP or ST will take over from there, so the developers never come close to a synthesizable model. That won't matter to RTL-challenged developers, but others prefer the option of tinkering with the high-level model of a core.

HP and ST say their software-development tools will be superior to those provided by ARC Cores and Tensilica, and they claim their VLIW processors will be more scalable and deliver much higher performance. Those claims (among others) remain to be proved. What isn't in doubt is the ongoing trend toward more flexibility and customization in embedded-processor design, which is giving application developers more influence over decisions once made exclusively by CPU architects.