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EMBEDDED MARKET BREAKS NEW GROUND

Network Processors, Configurable Cores, New Architectures Are Key Trends

By Tom R. Halfhill {1/17/00-01}

While translucent blue plastic was radical enough to rejuvenate sales and inspire widespread copycatting in the PC market, embedded-system designers in 1999 were inventing completely new products and dramatically improving existing ones. It was a year of

proliferation, innovation, and diversity, not imitation and consolidation.

The unprecedented growth of LANs, the Internet, and wireless telephony spawned a new generation of network processors—chips that are highly optimized for the special demands of network infrastructures. Some of those processors from Intel, IBM, C-Port, and other vendors are using technology rarely seen before, such as chip multiprocessing (CMP). Other network processors, like Motorola's "NetDSP," are designed to handle new services, such as digital filtering for voice-over-IP (VoIP) communication.

In 1999, embedded chips penetrated even deeper into our lives, appearing in everything from portable MP3 music players to barking robotic dogs. The explosion of "smart" products is driving the embedded market in remarkable new directions—such as the configurable architectures from ARC Cores and Tensilica that give system engineers a degree of design freedom that was formerly the exclusive domain of CPU architects.

Another measure of this frenzy is that the industry announced more new instruction sets for the embedded market in 1999 than we've seen for the PC market in the past 15 years. Some of those instruction sets overhauled architectures that were originally designed for PCs and workstations—such as PowerPC's Book E, from IBM Microelectronics and Motorola, and MIPS32 and MIPS64, from Mips Technologies. Hitachi and STMicroelectronics announced SH-5, a major enhancement of Hitachi's popular SuperH embedded architecture.

Still other architectures broke completely new ground: Fujitsu's FR-V and Sun Microelectronics' MAJC are based on cutting-edge VLIW technology. And we're not even counting instruction-set extensions like Motorola's AltiVec, Mips's MIPS-3D, Lexra's Radiax, and SandCraft's Vector3D, or the first implementations of new DSP architectures, such as StarCore's SC140 and Analog Devices' TigerSharc.

Sega's Dreamcast, powered by Hitachi's SH7750 processor, hit the U.S. market in September and immediately established itself as the most powerful home video-game console on the market. But Sony and Toshiba demonstrated a MIPS-based chip set for Sony's future PlayStation 2 that promises to deliver even greater performance. Not to be outdone, Nintendo announced that its next-generation game console will use a new PowerPC chip designed by IBM. The significance of the video-game arms race goes far beyond entertainment. These machines are powerful personal computers in disguise, capable of usurping the role of conventional PCs for many home users. They parallel the development of advanced set-top boxes that can also run many common PC applications.

As a new millennium dawns, the embedded market finds itself on the verge of a growth spurt that has no end in

sight. Aggregate unit sales were up 13% through October, according to Cahners In-Stat, and we estimate that the biggest gains were made by ARM and PowerPC (see Figure 1). All of the major trends pushing the industry forward in 1999 will gain momentum in 2000 and beyond.

Network Processors Take Off

The hottest trend in 1999 was network processors. It's a nebulous category, though, and numerous companies tried to jump on the fast-moving bandwagon. Even the definition is debatable.

For now, we'll define a network processor as any microprocessor for network-infrastructure applications that has significant logic dedicated to packet routing or processing. This excludes the microcontrollers and processors intended primarily for end-node devices—such as network printers, network-interface cards, and Internet-enabled cell phones—as well as the auxiliary chips that carry out narrow networking tasks, such as ATM framing.

Like anything new, network processors didn't suddenly appear out of nowhere. Motorola's QUICC (quad integrated communication controller) and PowerQuicc chips have been combining CPU cores with network-protocol engines since the early 1990s (see *MPR 5/10/93-03*, "68360 Provides Sophisticated Communications"). More specialized chips, such as ATM framers, have been around for years too.

The network processors announced in 1999 are applying much higher levels of integration to satisfy the growing demand for switching capacity and higher-layer packet-handling services, such as virtual private networking and TCP termination. They are also enabling new features, such as digital filtering for VoIP packets and quality-of-service routing based on packet priorities. Their specialized instructions, I/O buses, and on-chip memories are designed to outperform general-purpose RISC processors in networking applications while saving customers the time required to develop custom ASICs. They are also programmable devices that adapt more easily to new demands, unlike some high-performance but fixed-function ASICs.

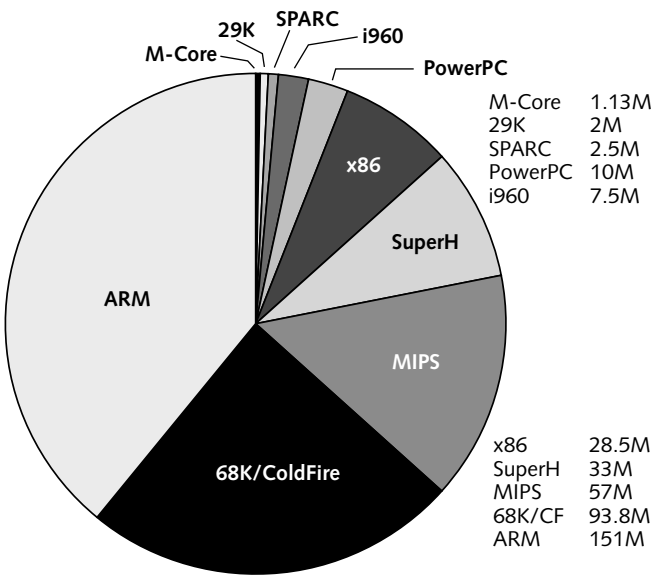

Figure 1. These 1999 unit sales are based on vendor reports and MDR estimates. The biggest news: ARM unit sales surpassed those of 68K/ColdFire chips, making ARM the best-selling 32/64-bit embedded architecture in the world.

Intel made headlines in September by announcing its first network processor, the IXP1200. Actually, the chip is being sold by Level One—a recent Intel acquisition that has more experience in the networking market. But in a strange turn of events, neither company was primarily responsible for designing the chip.

That credit goes to Digital Semiconductor, another Intel acquisition, which was secretly working on the IXP1200 long before Intel knew anything about it. In other words, one of the most important new processors of the year fell into Intel's lap as a result of Digital's ill-fated patent-infringement lawsuit against Intel (see *MPR 11/17/97-01*, "Digital Sells Its Chip Business"). That's why we name the IXP1200 the **Best Grab-Bag Prize** of 1999, and Digital Semi wins the **Most Productive Defunct Company** award.

Serendipity was never sweeter. The IXP1200 integrates a StrongArm core with six RISC microengines, an SDRAM controller, an SRAM controller, a PCI interface, and a high-speed bus that connects to additional IXP1200 chips in multiprocessor configurations. Clocked at a conservative 166 MHz, the IXP1200 can nevertheless perform layer-3 routing for 2.5 million 64-byte packets per second, according to Intel's estimates.

To steal some of Intel's thunder, C-Port and IBM announced their own network processors at about the same time. C-Port's C-5 integrates 16 channel processors that receive, process, and transmit cells and packets, while five on-chip coprocessors handle table lookups, memory management, and other chores. IBM's Network Processor has a PowerPC 40x core and 10 smaller RISC cores for executing similar tasks.

All these chips are scheduled to ship in 2000—Intel's and C-Port's in 1Q00, and IBM's in midyear. They will no doubt be joined by many others. Some other new chips that fall into this broad category are Motorola's PowerQuicc MPC855T, a PowerPC-based device, and Motorola's MSC8101, a StarCore SC140–based DSP. The MSC8101 is notable for being the first implementation of the StarCore architecture, jointly developed by Motorola and Lucent.

By integrating a powerful DSP with a coprocessor module extracted from Motorola's MPC8260 PowerQuicc II, the MSC8101 can analyze a data stream and perform digital filtering on selected packets, such as those containing VoIP data. It can also perform segment-and-reassembly (SAR) operations on ATM cells. Motorola calls the MSC8101 a NetDSP, which is clever enough to win our **Best New Buzzword** award.

Need a Chip? Add Water and Stir

No summary of the embedded market would be complete without taking notice of another major trend: configurable processors. Despite the widening variety of off-the-shelf embedded chips, licensable cores, SOCs, and ASSPs, sometimes a product designer needs a solution that's custom-tailored for a specific problem. That usually means licensing a core and spinning an ASIC, but there are times when even the available cores aren't quite good enough.

That's why ARC Cores, Cradle, Tensilica, Triscend, and other companies are offering design-a-chip kits. At Embedded Processor Forum, ARC Cores released the third version of its configurable 32-bit processor core, which lets customers use a graphical tool called ARChitect to add new instructions, define new condition codes, and modify the register file, among other things. The ARC 3 core comes with some optional DSP extensions that significantly improve on the basic DSP capabilities in the ARC 2 core. ARChitect, which can be freely downloaded from the company's Web site, guides customers through the design process without requiring them to manipulate the actual HDL code. When they're done tweaking, ARChitect generates a Verilog or VHDL model of the design, ready for porting to silicon.

Tensilica tries to make the job even easier by providing a Web-based tool similar to ARChitect. It's almost like ordering a book on Amazon.com. By selecting options on a series of HTML forms, customers can rapidly configure a custom core and take delivery of a verified Verilog model, also ready for silicon. Tensilica imposes some restrictions that ARC Cores does not—for example, new instructions must execute in a single cycle—but both companies shield customers from delving into the hairy details of HDL code.

Triscend is taking a somewhat different approach (see *MPR 11/16/98-02*, "Triscend E5 Reconfigures Microcontrollers"). Instead of giving customers control over the core, Triscend integrates an 8051-compatible MCU with reprogrammable logic for the purpose of emulating peripherals. This lets customers design a field-upgradable SOC for specific applications. Triscend even supplies a design tool that looks like Visual Basic for SOCs. Adding a common peripheral like a UART to the chip is as easy as dragging an icon from a toolbar.

Reprogrammable logic makes Triscend's solution too expensive for high-volume applications, but it's ideal for low-volume, highly specialized SOCs. Triscend shipped its first chip in the fall and plans to deliver a more powerful version with an ARM core in 2000.

Because ARC Cores was delivering configurable cores first, has more licensees, and offers more design flexibility, we name its V3 core the **Most Malleable Microprocessor** of 1999. Tensilica's HTML-based design tool wins the company a prize for inventing the **Best New Use for the Web**. And Triscend gets a trophy for coming up with the **Best New Use for an Eight-Bit Microcontroller**.

Best Embedded Processor 1999

To reflect the diversity of the embedded market in 1999, we nominated seven chips for our **Best Embedded Processor** award—more chips than in any other award category. Our nominees:

- **ARC Cores V3**, the latest example of the company's pioneering configurable core.
- **C-Port C-5**, a network processor based on an innovative new chip-multiprocessing (CMP) architecture.
- **IBM PowerPC 405GP**, an SOC that implements the 405 core, CodePack code compression, and IBM's CoreConnect on-chip peripheral bus.
- **Intel/Level One IXP1200**, another network processor based on a new CMP architecture.
- **Motorola DSP56690**, a highly integrated SOC that supports all international wireless-telephony standards.
- **Sony/Toshiba Emotion Engine**, a powerful MIPS-based chip for the PlayStation 2 video-game console.
- **Tensilica XTensa**, a new configurable-processor core and tool chain.

Picking a winner from this list was difficult because they represent so many disparate categories. Finally we settled on the **Sony/Toshiba Emotion Engine**. We were impressed by its all-out pursuit of performance for a high-volume consumer product that has the potential to replace PCs for some home applications. We also recognize its companion chips (the Graphics Synthesizer and the MIPS-based I/O processor) as part of the total PlayStation 2 solution.

Finally, there's Cradle Technologies, which announced a configurable chip that nearly defies description. Cradle's Universal Microsystem (UMS) combines a parallel array of microprocessor and signal-processor cores with programmable logic and I/O protocol engines—all connected to a 64-bit global bus that runs at 640 MHz. Cradle claims the UMS makes it possible to implement high-performance chips that are faster, easier, and cheaper to design than ASICs. "The ASIC as we know it is dead," the company declares.

Those claims are yet be proved—Cradle expects to deliver the first UMS chips in 1Q00—so they justify our **Hottest Hype** award. Even so, we believe Cradle's innovative architecture is a harbinger of more configurable processors in the future.

Teaching Old Dogs New Tricks

The most impressive news in 1999 was the proliferation of new instruction-set architectures (ISAs). The embedded market still has a Wild West flavor that's been missing from the PC market since the early 1980s. Without an operating-system monopoly, a dominant microprocessor architecture,

Key Embedded Events of 1999

- **Alchemy Microprocessor Design Group** was launched by some former Digital Semiconductor engineers who designed the StrongArm. Alchemy is working on a new MIPS processor core (*MPR 4/19/99-en*, p. 5).
- **Alliance Semiconductor** announced a "network processor" for routers that's 1% logic and 99% embedded memory (*MPR 8/2/99-02*, p. 14).
- **AMD** began sampling the Elan SC520, a new variant of its x86-compatible integrated processors for embedded applications.
- **Analog Devices** announced the ADSP-TS001, the first implementation of its TigerSharc architecture (*MPR 12/6/99-en*, p. 5); announced the ADSP-219x, a new 16-bit fixed-point DSP core that adopts Arm's Advanced Microcontroller Bus Architecture (*MPR 10/25/99-en*, p. 5); and announced a partnership with Intel to develop a new high-performance DSP architecture (*MPR 2/15/99-msb*, p. 4).
- **ARC Cores** released ARC 3, a new version of its configurable 32-bit processor core with better DSP instructions, larger on-chip memories, more power-saving features, and an improved C/C++ tool chain (*MPR 5/31/99-04*, p. 16).
- **Arm** introduced the ARM9E core with DSP extensions (*MPR 6/21/99-03*, p. 11), licensed the core to LSI Logic and Lucent (*MPR 7/12/99-en*, p. 7), and announced the first two ARM9E designs: the ARM966E-S and the ARM946E-S (*MPR 8/23/99-en*, p. 5).
- **C-Port** began sampling the C-5, a high-end network processor for routers, and helped form CPIX, an industry forum that will develop common APIs for different network processors (*MPR 10/6/99-en*, p. 18).
- **Cirrus Logic** began shipping the Maverick EP7212, an ARM720T-based integrated chip for handheld computers and portable Internet-audio devices (*MPR 11/15/99-03*, p. 22).
- **Cradle Technologies** unveiled the Universal Microsystem, a unique chip that integrates a parallel array of microcontrollers and DSP cores with programmable logic and I/O protocol engines (*MPR 10/6/99-03*, p. 26).
- **DSP Group** released Teak, its third-generation licensable DSP core (*MPR 8/2/99-05*, p. 19).
- **EEMBC** (EDN Embedded Microprocessor Benchmark Consortium) released a preliminary version of its benchmark suite, along with preliminary results (*MPR 6/21/99-01*, p. 1).
- **Fujitsu Microelectronics** introduced FR-V, a new VLIW architecture, and announced two FR-V cores, the FR300 and FR500 (*MPR 8/2/99-04*, p. 18).
- **Hewlett-Packard** (with STMicroelectronics) announced a partnership to develop customizable VLIW-based embedded processors that are programmable in C.
- **Hitachi** (with STMicroelectronics) unveiled SH-5, a new 64-bit SuperH architecture, and announced the SH8000, an SH-5 SOC (*MPR 10/6/99-04*, p. 20); introduced the SH7751, a variant of the CPU in Sega's Dreamcast videogame console (*MPR 6/21/99-02*, p. 10).
- **IBM Microelectronics** (with Motorola) overhauled the PowerPC architecture with the new Book E definition (*MPR 5/10/99-02*, p. 9); announced the first Book E implementation, the PowerPC 440 (*MPR 10/25/99-01*, p. 6); announced that Nintendo's next-generation game console will use an IBM PowerPC processor (*MPR 5/31/99-en*, p. 5); began sampling the PowerPC 405GP (*MPR 7/12/99-03*, p. 8); introduced CoreConnect, a freely licensed on-chip bus (*MPR 7/12/99-03*, p. 8); and announced a PowerPC-based network processor (*MPR 10/6/99-en*, p. 18).
- **IDT** unveiled the RISCore 64600, its third 64-bit MIPS-compatible core for high-end applications (*MPR 9/13/99-en*, p. 11); and released the RC64574 and RC64575, two MIPS-compatible 64-bit processors based on the RC5000 core (*MPR 8/23/99-04*, p. 18).
- **Infineon** (formerly Siemens) began manufacturing the first TriCore-based DSP, a 32-bit fixed-point superscalar design (*MPR 4/19/99-02*, p. 12).
- **Intel** announced a second-generation StrongArm design (*MPR 5/10/99-01*, p. 1); began sampling the IXP1200, a network processor to be sold by subsidiary Level One (*MPR 9/13/99-01*, p. 1); introduced a new StrongArm-1 integrated processor, the SA-1110, with a companion chip, the SA-1111 (*MPR 4/19/99-03*, p. 15); and bid $1.6 billion to acquire DSP Communications (*MPR 11/15/99-msb*, p. 4).
- **Lexra** rolled out three new soft cores: the LX4180 (*MPR 1/25/99-en*, p. 9), the LX4280 (*MPR 8/2/99-en*, p. 13), and the LX5280 with Radiax DSP extensions (*MPR 5/10/99-en*, p. 5); offered Radiax for free to MIPS licensees (*MPR 8/23/99-05*, p. 19); licensed embedded-DRAM technology from MoSys (*MPR 3/8/99-en*, p. 15); and was sued again by Mips Technologies (*MPR 11/15/99-en*, p. 16, and *MPR 12/6/99-03*, p. 14).
- **LSI Logic** bought ZSP Corp., a DSP startup (*MPR 8/2/99-en*, p. 13); licensed the ARM9E core (*MPR 7/12/99-en*, p. 7); and began designing an SOC for set-top boxes around SandCraft's new SR1-GX core (*MPR 7/12/99-04*, p. 10).
- **Lucent** introduced the DSP16410, which fits two DSP16000 cores on a single chip (*MPR 3/29/99-en*, p. 9); and announced (with Motorola) the SC140, the first Star-

Core DSP architecture (*MPR 5/10/99-03*, p. 13).

- **Massana** revealed the FILU-200, a synthesizable DSP coprocessor core that interfaces to a CPU's memory bus and includes prewritten C function libraries for common DSP applications (*MPR 10/25/99-en*, p. 5, and *MPR 11/15/99-02*, p. 17).
- **Mips Technologies** announced two new instruction-set architectures for embedded processors—MIPS32 and MIPS64—along with its first synthesizable processor cores, the 4K series (*MPR 5/31/99-05*, p. 18, and *MPR 10/6/99-en*, p. 25) and 5K series (*MPR 10/25/99-05*, p. 22); formed a partnership with Chartered Semiconductor to offer customers simplified MIPS licenses and cores preported to an IC process (*MPR 7/12/99-en*, p. 7); introduced MIPS-3D, a set of 13 new instructions for 3D graphics (*MPR 8/23/99-en*, p. 5); signed Texas Instruments as a licensee (*MPR 3/8/99-en*, p. 5); and filed a patent-infringement lawsuit against Lexra (*MPR 11/15/99-en*, p. 16, and *MPR 12/6/99-03*, p. 14).
- **Motorola** (with IBM Microelectronics) overhauled the PowerPC architecture for embedded applications with the new Book E definition (*MPR 5/10/99-02*, p. 9); announced the MSC8101, a StarCore SC140–based DSP for networking applications (*MPR 10/6/99-03*, p. 19); began producing the PowerQuicc MPC855T, a PowerPC-based network processor (*MPR 7/12/99-en*, p. 7); introduced the PowerPC 755 and 745, improved versions of the 750 and 740; rolled out faster and more-integrated versions of its 683xx-series DragonBall chips (*MPR 11/15/99-en*, p. 14); and began sampling the DSP56690, a dual-core chip that supports all worldwide cellular-telephony standards (*MPR 12/6/99-04*, p. 18).
- **National Semiconductor** sold Cyrix to Via (*MPR 7/12/99-02*, p. 5) but retained enough engineers and intellectual property to introduce the Geode SC1400, an SOC based on the x86-compatible MediaGX (*MPR 8/2/99-03*, p. 16).
- **NEC** and **Toshiba** renewed their MIPS licenses for 10 years (*MPR 1/25/99-en*, p. 9) and licensed the high-performance MIPS 20K Ruby core, which will be announced in 1H00.
- **Patriot Scientific** licensed its PSC1000 Java chip to Japan's Venture SystemLSI Assist Center, a government-funded body that helps Japanese technology startups (*MPR 4/19/99-en*, p. 5).
- **Philips** decided to stop making processors for handheld computers, focusing instead on MIPS processors for set-top boxes and digital TVs, as well as mixed-signal companion chips for embedded CPUs (*MPR 2/15/99-en*, p. 5); began manufacturing the TM-1300, the latest TriMedia processor (*MPR 8/2/99-en*, p. 13); and announced the NX-2600 and NX-2700, two new members of the TriMedia family for HDTV applications (*MPR 9/13/99-en*, p. 11).
- **QED** announced the RM7010, a 64-bit MIPS core to be manufactured in 2000 on IBM's 0.18-micron copper process. (*MPR 5/10/99-en*, p. 5).
- **SandCraft** taped out the SR1-GX, a MIPS-compatible core with DSP and multimedia extensions, and licensed it to LSI Logic, which is designing an SOC for set-top boxes (*MPR 7/12/99-04*, p. 10).
- **Sony** and **Toshiba** revealed the startling Emotion Engine and Graphics Synthesizer, a pair of embedded chips that will power Sony's next-generation PlayStation 2 videogame console (*MPR 4/19/99-01*, p. 1).
- **StarCore**, a Lucent-Motorola partnership, revealed its first DSP architecture, the SC140 (*MPR 5/10/99-03*, p. 13), and claimed that new optimized compilers will allow developers to write much of their SC140 software in C instead of assembly language (*MPR 12/6/99-en*, p. 5).
- **STMicroelectronics** (with Hitachi) unveiled SH-5, a new 64-bit SuperH architecture, and announced the ST50, an SH-5 SOC (*MPR 10/6/99-04*, p. 20); announced a partnership with Hewlett-Packard to develop customizable VLIW-based embedded processors.
- **Sun** unveiled MAJC, a new VLIW architecture designed for thread-level parallelism and chip multiprocessing (*MPR 8/23/99-03*, p. 13, and *MPR 9/13/99-02*, p. 12); announced the MAJC-5200, the first MAJC processor (*MPR 10/25/99-04*, p. 18); introduced the 400-MHz UltraSparc-IIe, a 64-bit processor for high-end embedded applications (*MPR 6/21/99-en*, p. 5); began shipping code for Jini, a Java-based technology intended to make it easier for smart devices to interact with PCs and networks (*MPR 3/29/99-03*, p. 10); and began offering free synthesizable models of its SPARC and PicoJava cores (*MPR 3/8/99-en*, p. 5).
- **Tensilica** introduced a configurable CPU architecture that lets ASIC designers add their own instructions and create customized chips by using a nifty Web interface (*MPR 3/8/99-02*, p. 12).
- **Texas Instruments** licensed the MIPS architecture (*MPR 3/8/99-en*, p. 5); licensed NEC's little-known V850 architecture; introduced two floating-point DSPs based on the 'C3x and 'C6x architectures (*MPR 3/29/99-en*, p. 9); and announced low-power versions of its 'C5000-series DSPs (*MPR 5/31/99-en*, p. 5).
- **Triscend** shipped the TE520, an SOC that combines an 8051-compatible microcontroller core with reconfigurable logic (*MPR 10/6/99-en*, p. 18).
- **Zoran** announced Muzichord, a 32-bit fixed-point synthesizable DSP core designed for next-generation digital-audio applications (*MPR 11/15/99-en*, p. 15).

or an entrenched software base to discourage them, embedded-processor architects have more freedom to discard old baggage and start afresh. One downside is that new ISAs usually require new development tools, and they impose a learning curve on embedded-system designers.

At Embedded Processor Forum in May, IBM and Motorola unveiled Book E, which revamps a RISC architecture whose embedded sales already far surpass its success on the desktop. We estimate that IBM and Motorola each sold about 5 million embedded PowerPC chips in 1999, which is roughly twice as many as they sold in 1998.

PowerPC processors built on the Book E definition will be backward compatible with 32-bit user-mode applications while gaining some valuable new capabilities. Improved 64-bit addressing is the most important feature, because future RAID controllers, routers, and switches will need 64-bit addressing to cope with rapidly expanding mass-storage systems and networks. Book E also streamlines the PowerPC's support for memory management, interrupts, and timers.

IBM didn't wait long to announce the first implementation of Book E: the PowerPC 440, which was described at Microprocessor Forum in October. The 440 is the first embedded-processor core to reach 1,000 MIPS with the Dhrystone 2.1 benchmark. At its nominal frequency of 555 MHz (in IBM's 0.18-micron copper CMOS-7SF), this out-of-order, two-way superscalar core wouldn't be out of place in a desktop system. It's nearly four times faster than IBM's new PowerPC 405GP and includes the first 128-bit version of IBM's CoreConnect, an on-chip peripheral bus.

Thanks to Book E and the 440, the PowerPC wins our **Most Improved Embedded Architecture** award for 1999, narrowly edging out MIPS32 and MIPS64.

The new MIPS instruction sets, like Book E, overhaul a desktop/server RISC architecture for the new realities of the embedded market. This was a necessary move after Mips separated from its parent company, SGI, which is struggling for survival in the workstation/server market. In 1999, Mips worked hard to put more distance between itself and SGI, announcing several new embedded cores to compete against its biggest nemesis, Arm. For successfully separating from SGI, Mips deserves our **Ejection Seat** award.

Mips introduced three new cores based on MIPS32—the first synthesizable cores ever offered by the company. (Another rival, Lexra, has introduced synthesizable cores that are 99% compatible with the MIPS architecture.) In October, Mips announced the first MIPS64 implementation—which is also the first synthesizable 64-bit processor core from any vendor.

Although the soft cores from Mips aren't nearly as configurable as the offerings from ARC Cores and Tensilica, they are based on a better-supported architecture and allow designers to exercise some control over the caches, registers, and MMUs. For instance, merely by changing one option (the MMU), an ASIC designer can determine whether or not the processor will run Windows CE.

The compromises inherent in the high-level design of a soft core inevitably limit performance, so Mips will announce a MIPS64-based hard core in mid-2000 that targets 1,000 Dhrystone MIPS. Known as the 20K Ruby, this core is also expected to implement the MIPS-3D extensions for 3D graphics. The first licensees are NEC and Toshiba. If all these cores are successful, Mips may qualify next year for our **Soft Landing** award.

Starting With a Blank Slate

Not content to revise existing instruction sets, the engineers at Hitachi, ST, Sun, and Fujitsu took a more aggressive approach by creating entirely new architectures. But Hitachi and ST did maintain backward compatibility with Hitachi's 32-bit SuperH when they jointly designed the 64-bit SH-5.

Despite a vastly expanded register file and instruction set, SH-5 supports all existing SuperH instructions and registers by deftly morphing old instructions into new ones at run time. This strategy preserves one of SuperH's greatest strengths: high code density. SH-5 has the power to tackle cutting-edge applications like next-generation game consoles and set-top boxes without abandoning its roots as a solid architecture for traditional embedded applications.

That's why SH-5 wins our **Best Collaborative Effort** award for Hitachi and ST, with bonus points for amiably sharing the credit and not sniping at each other during industry conferences.

Sun's MAJC (Microprocessor Architecture for Java Computing) caught everyone by surprise with its bold approach to VLIW, thread-level parallelism (TLP), and CMP. Sun believes the returns beyond four-way instruction-level parallelism (ILP) are too diminishing to justify wider architectures. Instead, MAJC integrates multiple cores on a single chip and assigns a different thread to each core. This approach bets heavily on exposing the TLP in multithreaded software—software that's relatively easy to write in Java, an inherently multithreaded language. But MAJC isn't Java specific and doesn't natively execute Java bytecodes, as so-called Java chips do. (Bytecode-native Java chips made little news in 1999, outside of a clever smart-card solution by Advancel.)

At Microprocessor Forum, Sun announced the first MAJC implementation, the MAJC-5200, which is claimed to have stunning floating-point and 3D graphics performance. If this chip finds its way into a set-top box or network computer, it could compete with PCs and game consoles at the same time. For pulling such an impressive rabbit out of the hat, MAJC wins our **Best New Architecture** award for 1999.

Sun isn't the only advocate of VLIW for embedded processing. Fujitsu's FR-V introduces a new VLIW instruction set that's divided into five subsets. By combining these subsets in different ways, Fujitsu can create optimized

processors for special applications. Customers can also design their own subsets of application-specific instructions. It's a step toward the fully configurable cores from ARC Cores and Tensilica.

In 1999, Fujitsu announced two FR-V cores: the FR300, which can execute two operations in parallel, and the FR500, which can execute four. But Fujitsu is withholding some crucial details of FR-V—such as the instruction set—until the IEEE International Solid-State Circuits Conference (ISSCC) in February, so it's difficult to evaluate. FR-V wins the **Most Mysterious New Architecture** award.

New Applications Spur Higher Integration

In 1999, few buzzwords were stretched as far as "system on a chip" (SOC). As new applications emerge, embedded designers must choose between cobbling a solution out of general-purpose parts or spending 12–24 months (and significant nonrecurring engineering funds) to develop custom ASICs. SOCs offer a more integrated solution that can get newfangled products to market before they're obsolete.

Trouble is, how much integration is enough? Some customers say that SOCs, like army uniforms, come in only two sizes—too big and too small. Architects have to figure out exactly what customers need, and often they must do it a year before the customers themselves know.

National Semiconductor led the charge toward higher integration by announcing the Geode SC1400. Although National calls the SC1400 an "information appliance on a chip," the device is so highly integrated that we're tempted to call it a "system on a chip on a system on a chip" (SOC^2).

National started with an updated version of the MediaGX chip set, which itself was an SOC for low-cost PCs when announced by Cyrix in 1995 (see *MPR 10/23/95-03*, "Cyrix GX Slashes System Cost"). To this x86-compatible core with integrated sound, graphics, and SDRAM control, National added a digital-video processor for MPEG decoding, a video-overlay processor that can merge graphics with video, and a whole slew of peripherals, including IDE, PCI, USB, Access Bus, UARTs, an infrared interface, power management, video input, xVGA video output, and NTSC/PAL TV output.

With a Pentium-class core clocked at 233–266 MHz, the SC1400 isn't nearly as fast as most RISC processors for information appliances. But it's fast enough for nongame applications, and it's x86 compatible, which will attract some customers. For taking a chip set that the PC market buried years ago and transplanting it into a trendy new SOC with unprecedented integration, we give National and the SC1400 our **Best Frankenchip** award.

IBM's PowerPC 405GP cannot match the SC1400's level of integration, but it is the most highly integrated chip in the PowerPC 400 series, and it excels in other ways too. It's the first implementation of the PowerPC 405 core, which at 200–266 MHz is about three times faster than the 401-series cores. It has the first implementation of IBM's CodePack, a memory-conservation technology that expands compressed executables on the fly (see *MPR 10/26/98-05*, "PowerPC Adopts Code Compression"). And it's the coming-out party for IBM's CoreConnect, an architecture-independent, freely licensed bus for integrating on-chip peripherals with cores.

The 405GP is well suited for its intended applications (Ethernet switches, low-cost routers, cable modems, network printers, cellular base stations, and so on). It has a 10/100-Mbit/s Ethernet interface, a PCI bus, a PC100 SDRAM controller, and sundry other peripherals. Scheduled to begin production in 1Q00, and competitively priced at $41 for the 200-MHz version, the 405GP wins our **Best Network-centric SOC** award.

Jump-Starting the Post-PC Era

SOCs for next-generation set-top boxes were also the craze in 1999. From their humble beginnings as cable-TV channel switchers and pay-per-view decoders, set-top boxes are evolving in so many different directions that it's more useful to think of them as peripherals for TVs. They include everything from satellite-TV receivers and WebTV-type appliances to video-game consoles and hard-disk video recorders.

Forget what you've heard about "convergence." For now, all these products are diverging. Maybe someday a single box will unite all those functions in a product that supports every applicable standard, but until then, embedded designers need specific solutions. In 1999, chip vendors tried to please them in numerous ways.

At Embedded Processor Forum, SandCraft announced the SR1-GX, an enhanced version of its MIPS-compatible SR-1 core. To meet the demands of a secret set-top box customer, SandCraft added an integer multiply-accumulate (MAC) unit, 16 new instructions for fixed-point DSP operations, a 64-bit FPU, 32 extra registers for single-precision floating-point numbers, and the Vector3D extensions, which consist of several new instructions for 32-bit single-instruction, multiple-data (SIMD) operations.

According to SandCraft, those improvements allow a 400-MHz SR1-GX to match or exceed the performance of an SR-1 core at 400–500 MHz. The lower clock rate will increase yields and reduce manufacturing costs—important considerations for a mass-market set-top box. LSI Logic has licensed the SR1-GX from SandCraft and is designing the SOC for the customer, which is expected to announce a product in 2H00.

SandCraft probably deserves a prize just for bending over backward to please the mystery customer, but we'll bestow an award on the fruit of SandCraft's labor: the SR1-GX is our **Best Licensable Core for Set-Top Boxes**.

Video Games Breed Monster CPUs

If a set-top box needs bleeding-edge game performance, however, the SR1-GX will find itself in very fast company

when matched against Hitachi's SH-4 and SH-5 processors or Sony's Emotion Engine. In 1999, those chips dramatically raised the barrier of entry to the home video-game market.

Hitachi reached the market first by shipping an SH7750 processor in Sega's Dreamcast console, which appeared in Japan in 1998 and the U.S. in September 1999. The SH7750 can sustain 1.2 GFLOPS at only 167 MHz. Although that's a bit less performance than the SR1-GX's 1.6 GFLOPS at 400 MHz, it's also a much lower clock frequency, which keeps costs down. For more-generic embedded applications, Hitachi also offers a variant of the SH7750 that has a narrower I/O bus, integrated PCI, and 42% less power consumption.

Despite those impressive efforts, Sony's MIPS-based Emotion Engine stands alone in this crowd. Designed with Toshiba, it's an over-the-top processor for Sony's next-generation PlayStation 2 console. At 300 MHz, the Emotion Engine executes 6.2 GFLOPS. Even desktop CPUs pale in comparison with this processor. For single-precision floating-point math—a critical part of 3D graphics—the Emotion Engine is twice as fast as Intel's 733-MHz Coppermine Pentium III with SSE, and it's 15 times faster than a 400-MHz Celeron without SSE.

Together with its companion chip, the Graphics Synthesizer, the Emotion Engine can calculate 75 million polygons and fill 2.4 billion pixels per second. That muscle doesn't come cheaply, however. Measuring 240 mm^2 in a 0.25-micron IC process, the 10.5-million-transistor Emotion Engine will cost more than $100 to manufacture, according to the MDR Cost Model. At 279 mm^2, the companion chip is even larger. Still, for taking a no-compromises approach to a high-volume consumer application in an intensely competitive market, we give the Emotion Engine our **Best Embedded Processor** award for 1999.

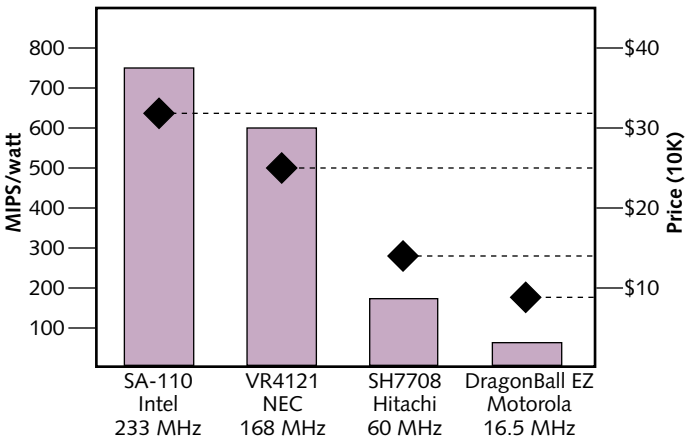

Figure 2. Four of the most popular embedded processors for mobile computers in 1999 span a 100-to-1 range in performance—a disparity that would never be tolerated in the PC market. In the embedded world, however, there's plenty of demand for a 2.7-MIPS chip that costs only $8.50 and consumes only 45 mW. Palm uses the DragonBall EZ for some of its handhelds.

Sony may not rule for long though. In 2000, Nintendo will reveal more details about its next-generation game console, code-named Dolphin. For that machine, IBM is developing a PowerPC-based CPU, code-named Gekko, and ArtX is working on a graphics coprocessor, code-named Flipper. (Won't somebody tell IBM that a lizard isn't a marine mammal?) Video games can soak up as much processing power as CPU architects can deliver, so there's no end to this trend.

Games aren't the only target. These powerful consoles can easily run other kinds of software, bringing some of the most popular PC applications (Web browsing, email, home shopping, online chat, discussion groups, instant messaging) into the living room. Consoles are much easier to use and maintain than PCs, and they cost less too. We think game consoles, recast as multifunction set-top boxes, will outsell PCs in the consumer market by the end of the next decade. PCs will be to set-top boxes what 35-mm single-lens-reflex cameras are to point-and-shoot cameras today—the choice of professionals and serious hobbyists, not average users.

More Choices for Embedded Designers

There was plenty of action in 1999 on other fronts as well. At Embedded Processor Forum, Intel announced that it will begin sampling a second-generation StrongArm core in early 2000. This was important for two reasons. There will finally be a successor to the first-generation StrongArm, which has steadfastly maintained its leading performance/power-consumption ratio for three years, despite its stasis in an antiquated 0.35-micron IC process. Second, it affirmed Intel's commitment to the StrongArm family, which was foolishly cast off by Digital in 1997.

The "SA-2" (our nickname, not Intel's) is supposed to hit 600 MHz while holding power consumption at 450 mW. To reach that clock frequency—astronomical for an embedded processor, and not too shabby for a desktop/server CPU either—Intel stretched the SA-1's five-stage pipeline to seven stages and made numerous other improvements.

Intel is manufacturing the SA-2 on a 0.18-micron IC process similar to the P858 process Intel uses for the Coppermine Pentium III. That means StrongArm will skip the 0.25-micron generation entirely, moving directly from Digital's old 0.35-micron process to a state-of-the-art production line. We expect the SA-2 to inherit the SA-1's leadership position with the best combination of performance and power consumption in 2000. It wins our **Most Likely to Succeed** award.

Intel wasn't the only busy Arm licensee in 1999. On the basis of sales reports for the first two quarters and run rates in the second half, Arm estimates that its licensees sold more than 150 million chips during the year. That's an impressive 3× increase over unit sales in 1998, which were 4× greater than unit sales in 1997. According to our estimates, it makes ARM the best-selling embedded-processor architecture in the world (in the 32/64-bit class), surpassing Motorola's

sales of 68K/ColdFire chips for the first time. It looks like Arm's policy of selling licenses to anybody who has a few million dollars and can spell "microprocessor" is paying off. And the future looks even brighter, thanks to some potentially high volume design wins, such as Nintendo's next-generation Game Boy, which appears in 2000.

To keep its licensees well armed against the competition, Arm updated the two-year-old ARM9 core by introducing the ARM9E, which adds 10 new DSP instructions. Although DSP extensions for embedded processors are spreading faster than Pokémon trading cards, Arm's first attempt at DSP—the separate Piccolo core announced in 1996—missed the mark. The ARM9E core does a much better job of integrating DSP functions.

Arm quickly followed up by announcing two ARM9E-based synthesizable cores at Embedded Processor Forum. The ARM966E-S substitutes tightly coupled SRAM for primary caches, and the ARM946E-S is a more conventional cache-based design. Arm's willingness to set aside Piccolo and play a different tune with the ARM9E earns our **Best Comeback** award.

Cirrus Logic faced the music in 1999, too, by introducing several chips that attempt to leverage the MP3 (MPEG-2 Layer 3) craze. This is a good example of how a new embedded application can prompt the development of a new integrated solution. Cirrus's Maverick EP7212 is an ARM720T-based chip with a digital-audio interface, an LCD controller, a DRAM controller, and some other integrated peripherals. It's designed for mobile devices that can download and play MP3 audio files from the Internet.

In 2000, we expect to see more application-specific standard products (ASSPs) such as Maverick. For demonstrating the foresight to bet on downloadable Internet audio, Cirrus Logic wins the **I Can See for Miles** award (with apologies to The Who). But if the MP3 fad flops, we'll replace the trophy with our **Don't Get Fooled Again** award.

Another busy company in 1999 was Lexra. Though barely two years old, the company introduced three new synthesizable cores, including one with DSP extensions. Lexra began offering the Radiax DSP extensions for free to MIPS licensees. That may have annoyed Mips Technologies, because Lexra doesn't have a MIPS license, even though its cores are 99% MIPS compatible.

In October, shortly after licensing negotiations broke down, Mips filed a patent-infringement lawsuit against Lexra—the second time Mips has sued Lexra in two years. For displaying such a magnetic attraction to each other, Mips and Lexra deserve our **Cutest Couple** award. They are advised to patch up their differences before they get strangled by Arm.

Is There Life After Y2K?

If you're reading this, at least some of the approximately five billion microprocessors and microcontrollers sold in 1999 are still keeping the world humming after January 1. More than 95% of those chips are in embedded systems.

Unlike the PC market, which quickly abandons CPUs that fall below a rising performance threshold, the embedded market grows by accretion. New chips don't necessarily replace old chips. There's always some embedded designer who can use a processor that costs only a few dollars and sips only a few milliwatts of power, no matter how slowly it runs or how creaky its architecture. As Figure 2 shows, even a cutting-edge embedded product like a Palm handheld computer can get by quite nicely with a chip that would be considered woefully obsolete in the PC market.

In 2000, we expect the trends of 1999 to gain even more speed, and we hope to see some new trends as well. The leading categories to watch are network processors for routers, high-performance CPUs for multifunction set-top boxes, ASSPs for hot consumer products (digital cameras, cell phones, MP3 players, toys), and configurable cores that shorten ASIC design cycles.

Prime companies to watch: Intel, Arm, and Mips. Intel's days of focusing almost exclusively on PCs are over. While Intel is pushing strongly into the server/workstation arena with IA-64, it's also gaining ground in the embedded market with newly acquired or licensed architectures—IXA (represented for now by the IXP1200) and ARM. In 2000, Intel and Analog Devices (ADI) will announce a jointly developed DSP architecture. It's obvious that Intel is no longer content to offer embedded customers little more than hand-me-down x86 chips and the antiquated i960. Like a sleeping giant, Intel has awakened to fresh opportunities in the embedded market, and the company is no longer a captive of the not-invented-here syndrome.

Arm is worth watching because it has become the leading supplier of high-performance embedded processor cores and has the most impressive stable of licensees. Many cell phones use ARM chips, and wireless telephony is a high-growth market. This will put more pressure on Mips as a prime competitor for licensable cores. Design wins like the PlayStation 2 should boost Mips's fortunes in 2000.

Be prepared for some surprises too. There might be some new solutions for improving the performance and reducing the memory requirements of embedded Java, and the open-source movement that's rapidly gaining ground in the PC/server markets could gain a foothold with embedded versions of Linux as well. It will take more than a calendar change to derail this train.