SiByte Licenses MIPS for Network Processor

More refugees from Digital Semiconductor have surfaced, and they're working on a MIPS-based network processor. Their Santa Clara–based startup, SiByte, recently licensed the MIPS64 instruction-set architecture from Mips Technologies (see MPR 5/31/99, p. 18).

SiByte was founded in 1998 by Dan Dobberpul, Amarjit Gill, and Leo Joseph. Dobberpul, SiByte's president and CEO, was responsible for the design of Alpha, StrongArm, MicroVAX, and PDP-11 processors at Digital. Gill, who is vice president of sales and business development at SiByte, was the director of sales at Digital. Joseph, SiByte's vice president of marketing and operations, was Digital's marketing manager for StrongArm. SiByte currently has about 65 employees, mostly engineers, working on a 64-bit processor core known as the SB-1.

Ironically, the first SB-1 chip will probably compete head-to-head against a similar processor also designed by former Digital engineers—the Intel/Level One IXP1200 (see MPR 9/13/99, p. 1)—as well as network processors from IBM Microelectronics, Motorola, C-Port, Sitera, and others. When Intel acquired Digital Semi in 1997, it inherited the IXP1200, which was already under development. SiByte's chip, though based on a different architecture, appears to be similar in concept and aimed at the same market.

By the end of 2000, SiByte plans to ship a processor that integrates multiple SB-1 cores on a single die for chip multiprocessing (CMP). Because SiByte's processor uses MIPS-compatible cores, it will present a familiar architecture to system designers and programmers. In contrast, some other network processors that do CMP are based on completely new architectures, at least in part. For example, Intel's IXP1200 has a StrongArm for general-purpose tasks plus six microengines for packet processing—and the microengines introduce a new RISC architecture that requires special development tools. C-Port's C-5 processor and IBM's Network Processor also introduce new architectures, though IBM's chip also has a PowerPC core (see MPR 10/6/99, p. 18).

All of these companies are aiming at the network-infrastructure market: routers, multiprotocol switches, line cards, and similar equipment. Today, those devices typically use general-purpose RISC processors and custom ASICs. Network processors can be more optimized for those applications than general-purpose CPUs, and they can save customers the considerable time and money required to develop an ASIC.

One company that SiByte apparently will not directly compete against is Alchemy Microprocessor Design Group, another startup founded by Digital refugees. Although Alchemy has also licensed the MIPS architecture, Alchemy engineers are working on a 32-bit core for low-power embedded applications. Alchemy's chip will probably compete against StrongArm, which Intel also inherited with its acquisition of Digital Semi.

Thus two separate groups of former Digital employees will be competing against their former products, now owned by Intel. It's too bad Digital couldn't do a better job of leveraging its in-house talent when it had the chance. —*T.R.H.*

Motorola Releases Specs for On-Chip Bus

As it promised six months ago, Motorola's semiconductor products sector *(http://mot-sps.com/)* has released the specifications for its new core-independent on-chip peripheral bus, formerly known as IP Bus. The documentation will allow third parties to begin adapting their intellectual property (IP) to work with the freely licensed bus, although Motorola says it won't ship the code for bus bridges, bus monitors, and bus-functional models until early 2000.

Due to trademark conflicts, Motorola has changed the name of IP Bus to IP Interface (IPI). It defines a set of architecture, microarchitecture, and I/O-signal specifications that will allow designers to more easily integrate peripherals with CPU cores on system-on-a-chip (SOC) devices. By adapting their high-level Verilog or VHDL models to Motorola's specifications, designers can reuse their IP with different cores.

For now, those cores are all Motorola architectures: PowerPC, ColdFire, M-Core, and Motorola DSPs, with support for StarCore DSPs coming in the future. (IPI does not support the 68K, which Motorola is not promoting as a core for SOCs.) This is an important difference from IBM's CoreConnect, a similar on-chip bus specification (see MPR 7/12/99, p. 8). CoreConnect works with some non-IBM architectures, such as MIPS.

IPI and CoreConnect have other differences too. Motorola's solution is currently limited to bus widths of 64 bits, while CoreConnect extends to 128 bits (see MPR 10/25/99, p. 16); and IPI is not as far along as CoreConnect, which has already been designed into production silicon. Both bus specifications are freely licensed, so interested developers can evaluate and implement the technologies without paying hefty fees. —*T.R.H.*

Embedded Benchmarks Ready for Prime Time

EEMBC (EDN Embedded Microprocessor Benchmark Consortium) has released version 1.0 of two benchmarking suites: the automotive/industrial suite and the telecommunications suite. After many months of work, EEMBC's technical subcommittees have revised and approved the test programs in those suites. The tests are substantially the same as those in the preliminary 0.9 version of the benchmarks released in May (see MPR 6/21/99, p. 1).

Currently, EEMBC has 34 member companies, up from 29 last spring. More information is available on EEMBC's Web site at *www.eembc.org*. —*T.R.H.* M