Massana's DSP Coprocessor Bolts Onto CPUs

At this month's Microprocessor Forum, Massana described its new FILU-200 DSP coprocessor and announced that one of its customers is working on a broadband communications product for homes and businesses. Although the customer isn't ready to go public, the product will probably use the FILU-200 to support home-networking, xDSL, cable-modem, and analog-modem capabilities.

While many embedded-processor vendors are adding DSP extensions, Massana's solution is quite different: a synthesizable DSP coprocessor that attaches to the CPU's memory bus and is programmable with C function libraries. Massana *(www.massana.com)* claims this approach delivers better price/performance than either a discrete DSP or a general-purpose CPU that's powerful enough to emulate a DSP.

The FILU-200 typically runs at the same clock rate as the CPU core—up to 120 MHz at 0.25 micron or 150 MHz at 0.18 micron. With 30,000 gates, it occupies only 0.7 mm^2 of silicon in a typical 0.25-micron IC process. Massana says it's compatible with almost any embedded processor architecture, including MIPS, ARM, ARC, and SparcLite.

The FILU-200 has two multiply-accumulate (MAC) units with dual barrel shifters and adders, so it can execute two MACs per cycle. Massana says a 100-MHz FILU-200 can calculate a 256-point fast-Fourier transform (FFT) almost twice as fast as Lexra's 200-MHz LX5280 with Radiax extensions (see MPR 8/23/99, p. 19) or DSP Group's 130-MHz Teak DSP (see MPR 8/2/99, p. 19). At 100 MHz, the FILU-200 can calculate 200 million filter taps per second.

For easier programming, Massana offers C function libraries. One library encapsulates common DSP operations, while another is for the FFT-intensive G.Lite ADSL standard. A voice-over-IP library is under development. The general DSP and G.Lite libraries are available now, along with the FILU-200's RTL model and an instruction-set simulator.

Massana's approach to DSP integration gives designers a valuable third option beyond stand alone DSPs and RISC processors with DSP extensions. It complements the growing number of soft cores available from RISC vendors, and the FILU-200's gate count is a trifle in modern IC processes. The C function libraries make the FILU-200 attractive to developers who have little familiarity with DSP assembly-language programming and would rather keep it that way.

If customers find Massana's licensing terms equally attractive, the FILU-200 is a good solution. When time-to-market is paramount, however, a more conventional solution, based on a general-purpose CPU—with or without a discrete DSP—would eliminate the need to port a synthesizable core to silicon for an ASIC. Massana's prewritten function libraries will save development time on the software side, but similar libraries for regular DSPs and some embedded CPUs are available from other vendors. —*T.R.H.*

ADI Adopts AMBA for New DSPs

Analog Devices (ADI) unveiled a new DSP core at this month's Microprocessor Forum and announced that it will use Arm's Advanced High-Performance Bus (AHB) interface, which is part of the open-standard Advanced Microcontroller Bus Architecture (AMBA). The combination of AMBA and a synthesizable wrapper for the core allows ADI to design system-on-a-chip devices by integrating memory controllers, serial ports, telecommunications interfaces, and mixed-signal components.

The new core is the ADSP-219x, a 16-bit fixed-point DSP that's software-compatible with ADI's ADSP-218x family. It has a modified Harvard architecture—one bus fetches 24-bit instructions or 16-bit data operands from program memory while another bus fetches 16-bit operands from data memory. Hits in the instruction cache free up both buses for data transfers, so the DSP can fetch two 16-bit data operands in a single cycle. The instruction cache holds 64 instructions, is two-way set-associative, and follows a least-recently-used replacement policy. It's fully transparent, requiring no cache management by programmers.

To enable higher clock frequencies, the 219x has a new six-stage pipeline, twice as deep as the 218x's. Initial parts will run at 160 MHz, compared with 75 MHz for the fastest current 218x DSP (in a 0.25-micron IC process). Next year, ADI expects 219x DSPs to reach 300 MHz in a 0.18-micron process that has low-*k* dielectrics and copper interconnect layers. At 160 MHz and 0.25 microns, the 219x's power consumption is estimated to be 64 mW at 2.5 V.

The 219x can execute one multiply-accumulate (MAC) instruction per cycle. For higher-end applications, such as G.Lite processing in ADSL modems or channel partitioning in network routers, ADI plans to integrate two or four 219x cores on a single chip with up to 2 Mbytes of embedded DRAM. At 160 MHz, the quad-core chips will allow system designers to build Internet gateway equipment capable of handling 75 V.90 analog-modem channels or 100 voice-over-IP channels per square inch of board space.

Synthesizable DSP cores with comparable or higher performance are available from other vendors. Some examples are DSP Group's Palm (see MPR 9/14/98, p. 13) and Teak (see MPR 8/2/99, p. 19), and Infineon's Carmel (see MPR 12/28/98, p. 18). But the 219x isn't intended to be ADI's highest-performance DSP. That honor is reserved for the upcoming TigerSHARC architecture and for the fruit of ADI's collaboration with Intel.

Even so, the 219x delivers enough performance for many of today's industrial and telecommunications applications. ADI's adoption of the AMBA-AHB specification provides an extra measure of design flexibility, and the code compatibility with existing 218x-series DSPs should ease the transition for software developers. —*T.R.H.*