PowerPC 405GP Has CoreConnect Bus

IBM Offers Free Licenses to Make On-Chip Bus a New Standard

by Tom R. Halfhill

IBM's latest PowerPC processor, the 405GP, is a highly integrated system on a chip (SOC) with PCI, Ethernet, an SDRAM controller, and the first implementation of CodePack code compression. What's potentially more important is that IBM is using the 405GP to kick off the CoreConnect bus—an on-chip bus architecture for SOCs that IBM is offering free to all comers.

CoreConnect isn't exactly new. Over the past two years, IBM has designed more than 20 ASICs by using the bus to link CPU cores and macros from its Blue Logic library. Most recently, the bus appeared in a companion chip for PowerPC 600-series processors that Compaq is using as an I/O controller in RAIDs. What's new is that IBM has formalized the bus architecture for external use, has made it more CPU independent, and is freely licensing it to other chip companies, intellectual-property designers, and tool vendors.

IBM says the license has no strings attached: no up-front fees, no manufacturing fees, and no royalties. The first CoreConnect licensees are Cadence, Lexra, Mentor Graphics, Stellar Semiconductor, Summit Design, and Technical Data Freeway. IBM has formed a CoreConnect user group to help steer future development of the bus. Membership in the user group is free.

According to IBM, the user group isn't a standards committee and won't compete with the Virtual Socket Interface Alliance (VSIA), an industry group that's working to define standard interfaces for reusing intellectual property in ICs (see MPR 12/29/97, p. 15). But it's hard to ignore the overlap between CoreConnect and VSIA, not to mention ARM's Advanced Microprocessor Bus Architecture (AMBA), IDT's IPBus, Motorola's IP Bus (no relation to IDT's), and other on-chip interfaces vying for wider acceptance.

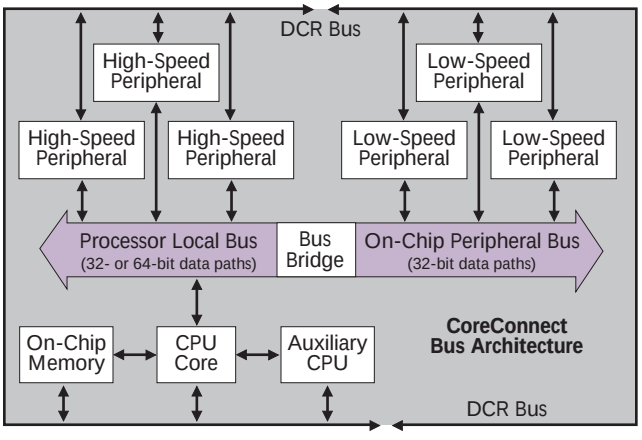

Figure 1. The CoreConnect architecture consists of three buses: the high-speed processor local bus (PLB), the lower-speed on-chip peripheral bus (OPB), and the device-control-register (DCR) bus.

Three Buses in One

As Figure 1 shows, CoreConnect actually has two main buses that separate higher- and lower-bandwidth peripherals, plus an auxiliary bus for the peripherals' device-control registers.

The fastest piece of CoreConnect is the processor local bus (PLB). It's a pipelined, split-transaction, fully synchronous bus that's comparable to the AMBA 2.0 high-performance specification (see MPR 11/16/98, p. 16). The PLB's independent read and write data paths can be 32 or 64 bits wide and are extendable to 128 or 256 bits in the future. They can transfer 16-, 32-, or 64-byte lines of data, and they support 8-, 16-, 32-, and 64-bit burst transfers as well as unaligned transfers. Under DMA control, they can handle buffered, fly-by, peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfers.

ASIC designers can attach up to 16 masters and any number of slaves to the PLB. The bus's maximum clock frequency, however, is limited by the number of attached devices, due to wire loads and the time it takes to arbitrate bus traffic. Highly integrated SOCs that would overload a single PLB with fast peripherals can use a second PLB to separate the masters and slaves. IBM has a macro called a PLB crossbar switch that allows the master and slave PLBs to communicate with each other through the bus arbiters.

Another macro bridges the PLB to the secondary CoreConnect bus, which is known as the on-chip peripheral bus (OPB). Designed to accommodate slower devices, the OPB is a fully synchronous bus with separate 32-bit address and data paths. It supports 8-, 16-, and 32-bit transfers and burst transfers. Dynamic bus sizing allows the OPB to work with slaves that have different data widths. The OPB bridge automatically breaks transactions into smaller pieces when accessing devices that can't handle larger chunks of data.

The slowest part of the CoreConnect architecture is the device control register (DCR) bus. It's a ring that connects the configuration and status registers of peripheral devices. It can handle one read or write every other cycle.

IBM's free license includes macros for the PLB arbiter, the OPB arbiter, the PLB-OPB bridge, and the bus monitors for both the 32- and 64-bit versions of CoreConnect. Test software will be supplied later. Additional macros, such as the PLB crossbar switch—and, of course, all those cool peripherals in the Blue Logic library that designers might want to hang on the bus—are available from IBM at the usual prices. Corporate largess goes only so far.

Price & Availability

IBM is sampling the PowerPC 405GP at 200 MHz now, with production scheduled for 1Q00. The price in 10,000-unit quantities is $41. IBM plans to sample the 266-MHz version by the end of the year and begin production in 1Q00. IBM hasn't announced the price for that part. For more information, go to *www.chips.ibm.com/products/powerpc/*.

Proving the Concept

The new PowerPC 405GP is a good advertisement for CoreConnect and Blue Logic. It's by far the fastest, most highly integrated chip in the PowerPC 400 series.

Other members of the 400 family have no on-chip peripherals and stroll at clock frequencies of 25–80 MHz. The 405GP is a genuine SOC that's loaded with useful peripherals. It's the first PowerPC chip based on the 405 core (see MPR 10/26/98, p. 26) and will zip along at 200–266 MHz.

Unlike earlier 400-series cores, which have minimal three-stage pipelines to conserve every milliwatt of power, the 405 has a more conventional five-stage pipeline that can reach higher clock frequencies. It also has a 16K instruction cache, an 8K data cache, 4K of additional on-chip memory in the form of SRAM, and a function unit that executes 24 different multiply-accumulate (MAC) instructions—a feature that no modern processor can do without, it seems.

As Figure 2 shows, the 405GP surrounds the 405 core with a wealth of on-chip peripherals, all joined together by the CoreConnect bus. In this implementation, the PLB is 64 bits wide and runs at 100 MHz—half of the core's 200-MHz frequency. A second version of the chip will have a 133-MHz PLB and a 266-MHz core.

The PLB connects the core to a DMA controller, an external bus-master controller, a PCI interface, an Ethernet interface, an SDRAM controller, and the CodePack decompression engine. The PCI version 2.2 interface can run synchronously at ratios of 1:1, 1:2, 1:3, and 1:4 of the PLB frequency, or it can run asynchronously at any ratio from 1:8 or higher, up to 66 MHz.

A dedicated DMA channel services the Ethernet interface, which supports 10- and 100-Mbit/s speeds (regular and Fast Ethernet) and connects directly to an external PHY chip. The SDRAM controller supports PC100 memory and has four chip selects, with 4M to 256M of memory per bank. It hooks into the PLB through the CodePack engine, which expands compressed executables on the fly.

The OPB runs at 50 MHz in the 200-MHz version of the 405GP or at 66 MHz in the 266-MHz version. It has a pair of 16550 UARTs, 23 general-purpose I/O ports, and an Inter IC (I^2C) controller.

In IBM's 0.25-micron five-layer-metal process, the 405GP has a die size of 49 mm^2. At 200 MHz and a core voltage of 2.5 V, the part consumes 1.1 W and executes 252 Dhrystone 2.1 MIPS. It's packaged in a 456-pin enhanced plastic ball grid array (E-PBGA).

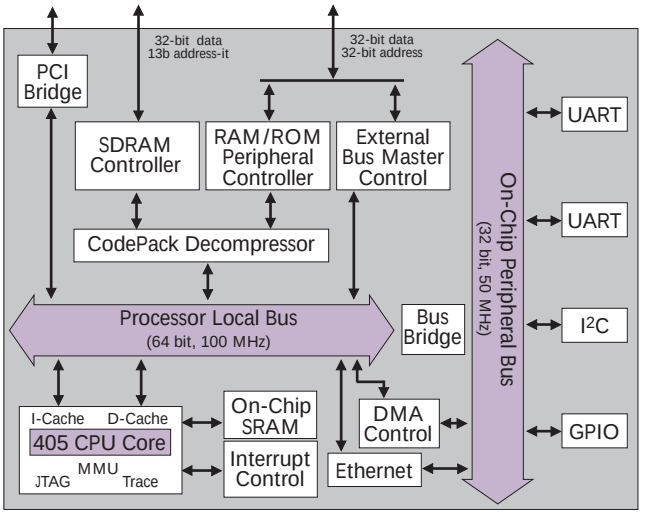

Figure 2. IBM's PowerPC 405GP is a fast, highly integrated system on a chip for network-capable embedded applications.

IBM designed the 405GP for Ethernet switches, low-cost routers, cable modems, network printers, base stations, remote-access devices, and similar applications. Its Ethernet port sets it apart from other embedded processors in this performance class that have a PCI bus and an SDRAM interface—such as Hitachi's SuperH 7751 and Motorola's 8240. At $41, the 200-MHz 405GP is competitively priced with the 167-MHz SH7751 ($39) and the 200-MHz 8240 ($55).

More Buses Than Greyhound

Everyone wants an industry-standard on-chip peripheral bus—as long as it's theirs. Why should IBM be any different?

It's not hard to see how IBM stands to gain from openly licensing CoreConnect. IBM has a library of cores and macros that already work with CoreConnect, and IBM's chip designers have years of experience with the bus. Other suppliers of cores and macros that adopt CoreConnect would have to catch up.

As proof that it's not trying to bulldoze the VSIA initiative, IBM says CoreConnect is architecture-neutral and complies with the general attributes that VSIA has defined so far. But when a company with the throw weight of IBM offers a free solution to a longstanding problem—integrating intellectual property on custom chips—that solution stands a fair chance of becoming a de facto standard, no matter what anybody else does.

As with most competitions of this sort, technical specifications are only one consideration. The winner—if, indeed, there is a winner—will likely prevail on the strengths of marketing muscle, mindshare, and moxie. What seems more likely is that all of the competing standards will fracture the market, delaying or derailing attempts to establish a neutral standard on which everyone in the industry can agree. M